FOSS for Free HW with Japanese technology process

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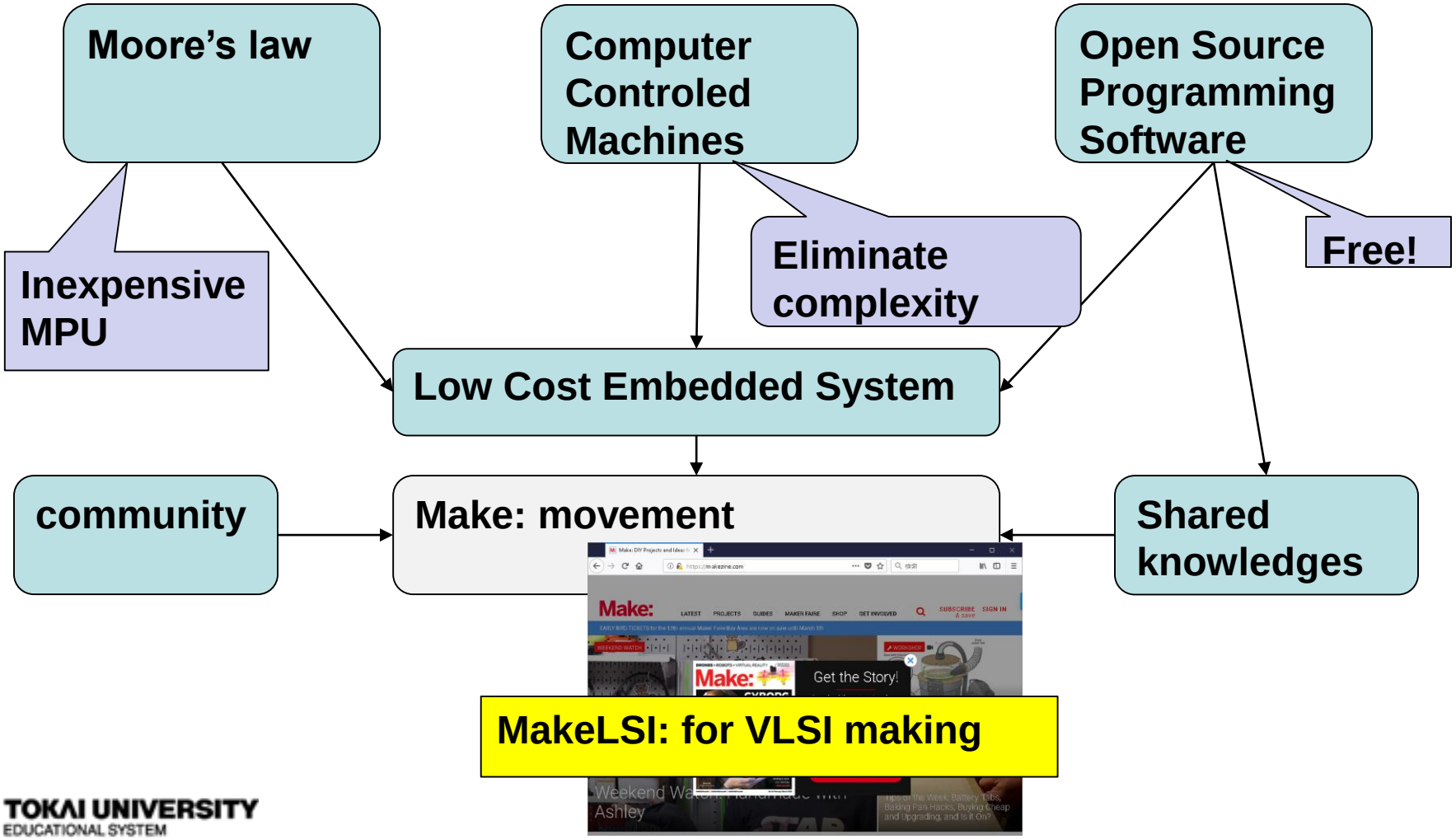
Outline

- Introduction and Motivation
- NDA less fabrications
- Our Idea
- Experiments
- Conclusion

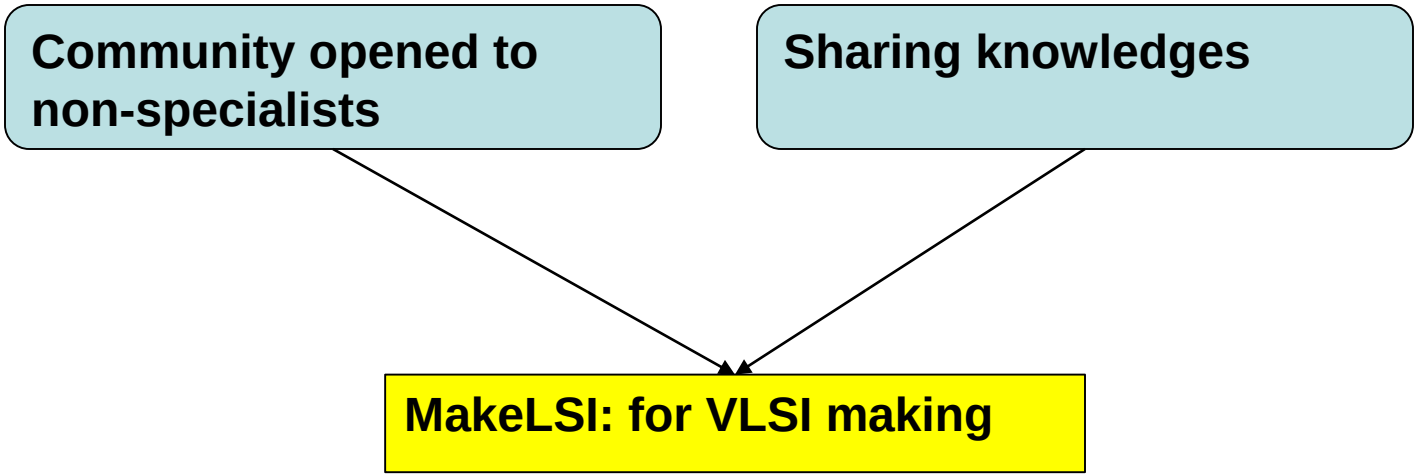
Introduction

- Make: movement attracts people
  - Diversity induces nice ideas
    - More people, more idea!
- We want Democratizing VLSI making
  - Induce diversity!
    - More people, more idea!
  - Not only digital but mixed signal!

More people, more idea
Make: movement



More people, more idea
Democratize VLSI Making



Problems in VLSI Design

Moore's law

Physic/chemical difficulty

System complexity

More transistors

Complex design

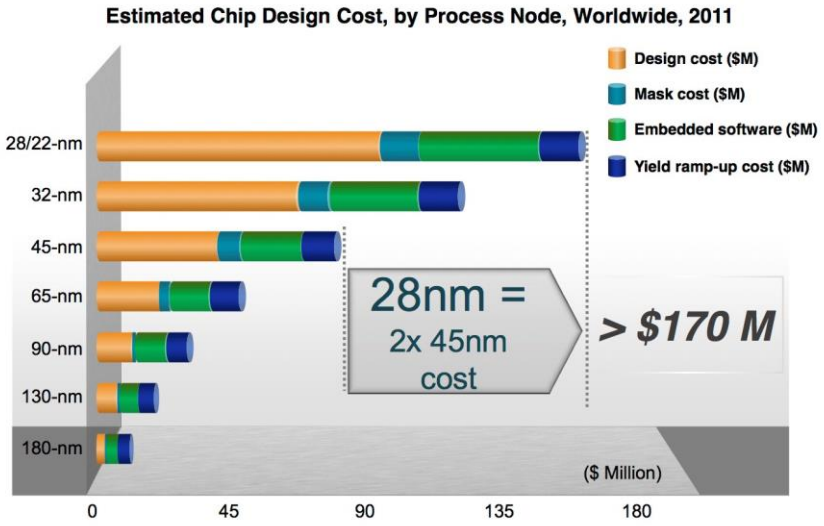
Complex fabrication

Complex software

Expensive EDA
Expensive fabrication

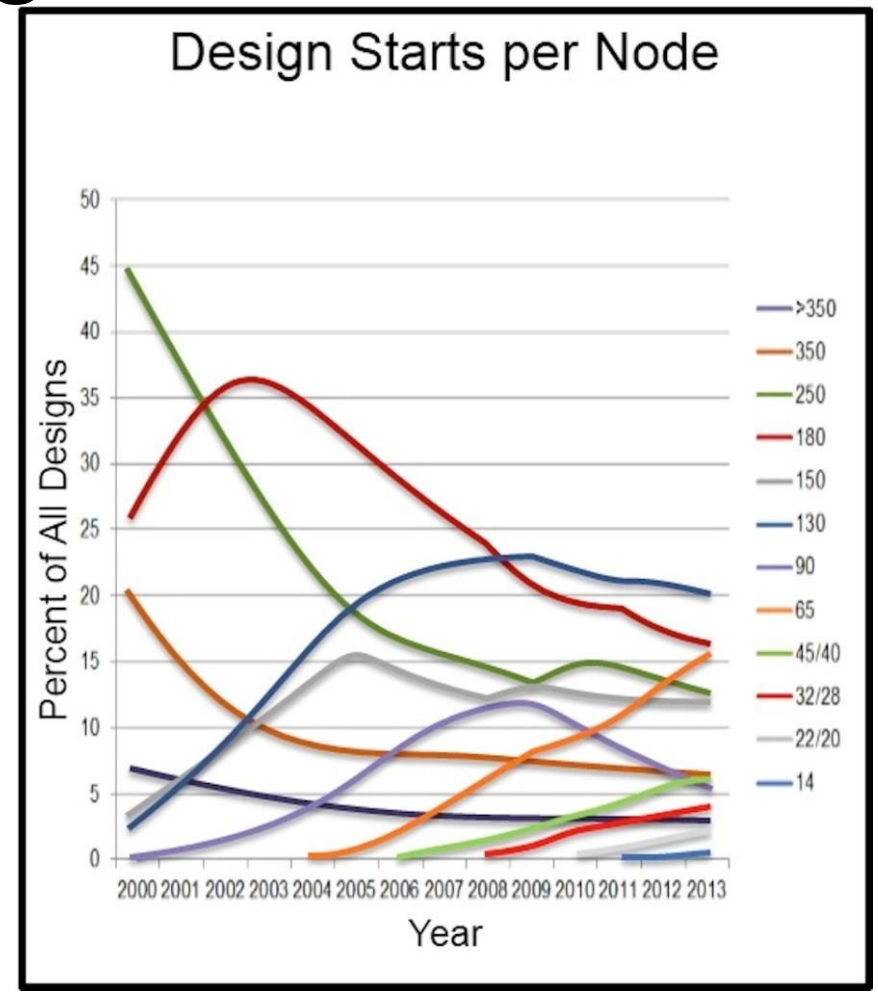
Q: Who can pay the cost?

Design Cost



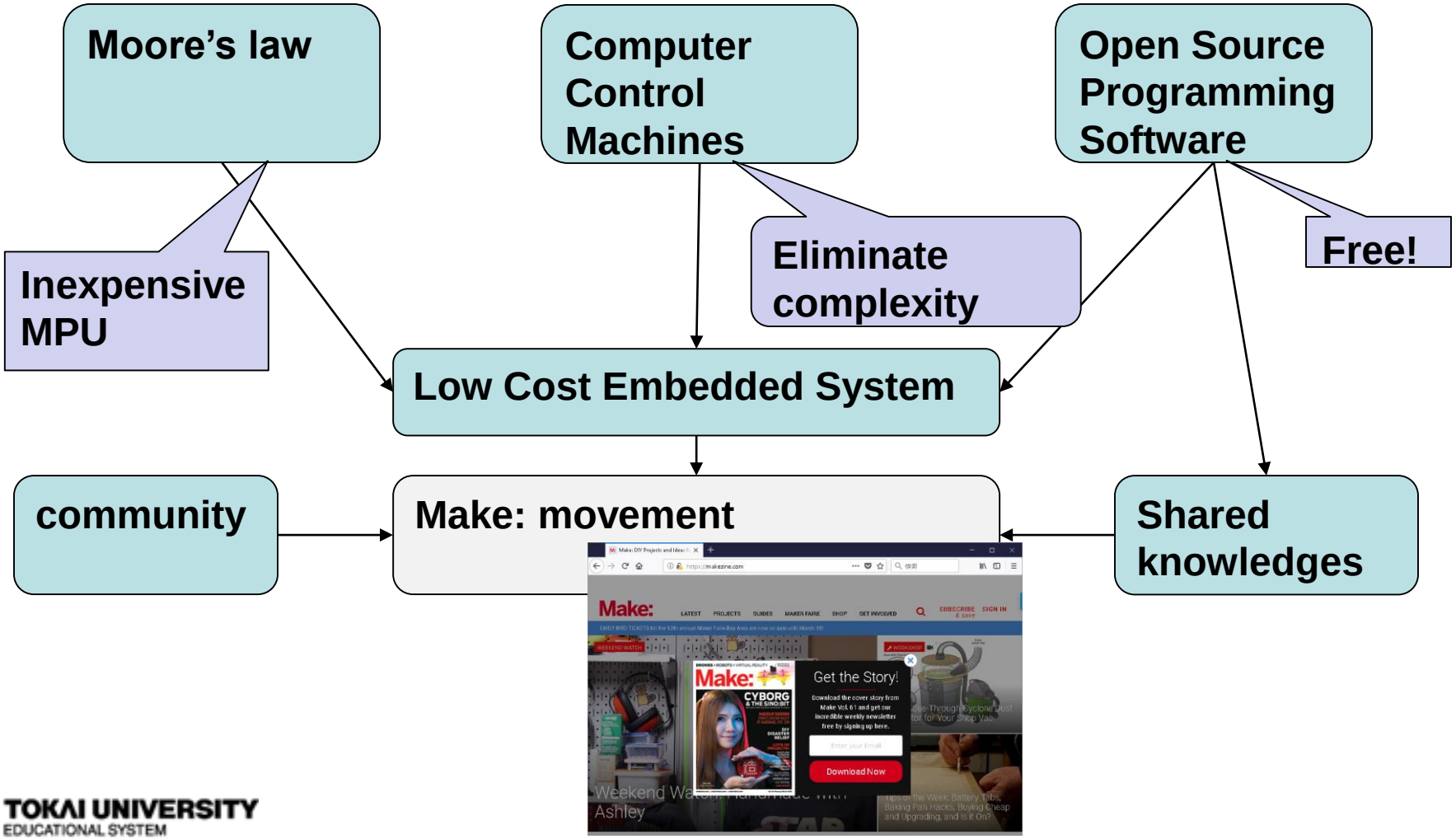
ASIC Design Trend

- Migration will not replace completely!
- Longtails for every processes.
- > 70% for >= 130nm in 2013
  - Estimation: 70% for >= 90nm in 2018.

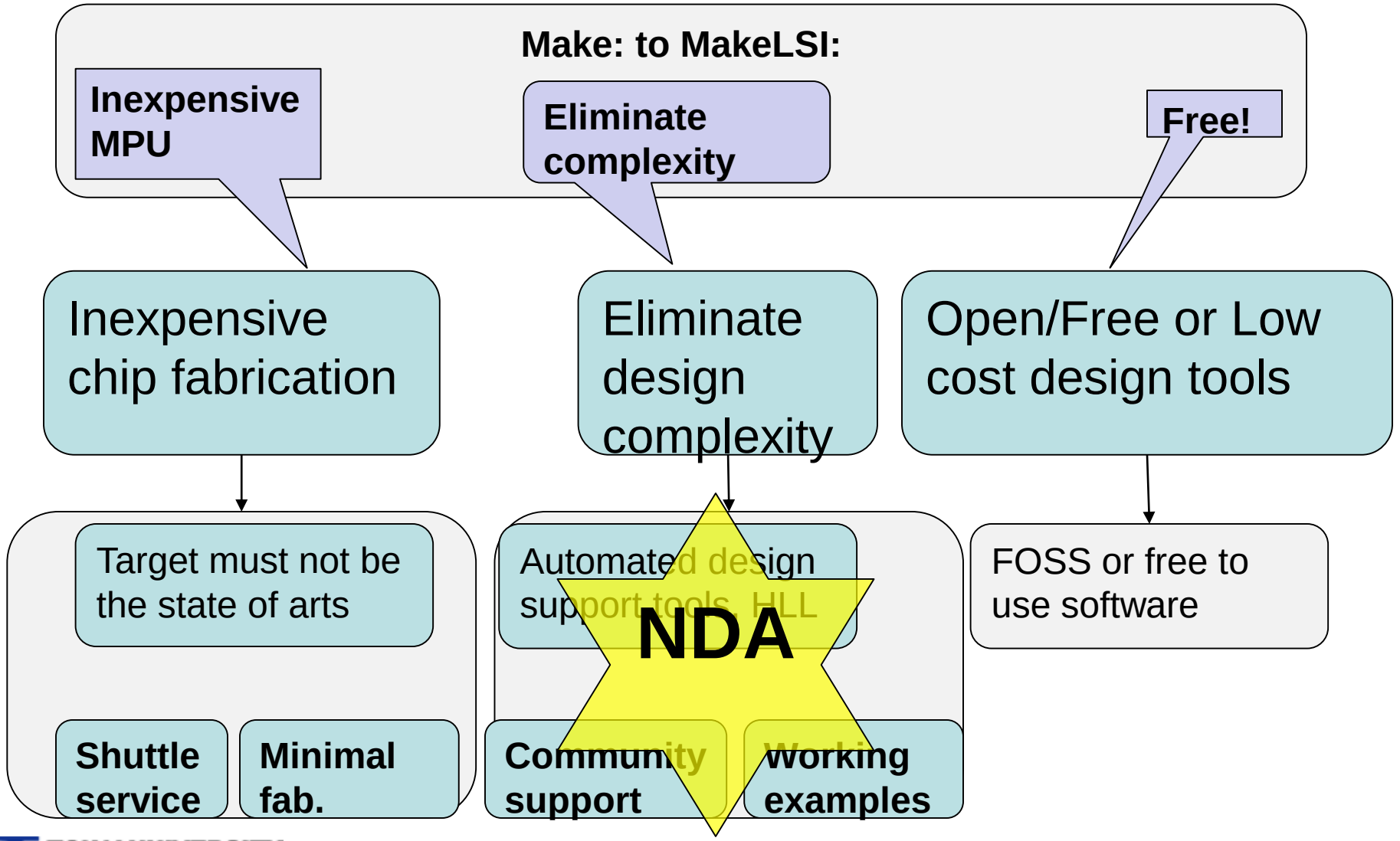


FPGA as ASIC Alternatives Past &Future, EETimes 2014

More people, more idea
Make: movement



Toward MakeLSI:



Motivation and Background

- NDA prevent us to share our experiences on VLSI design
  - cf. Open source software projects success with the sharing knowledge among contributors.
- Costly EDA tools prevent beginners to try even with a small design
- Most of FOSS EDA tools had stopped their developments.
- We want “Make:” movement for VLSI!

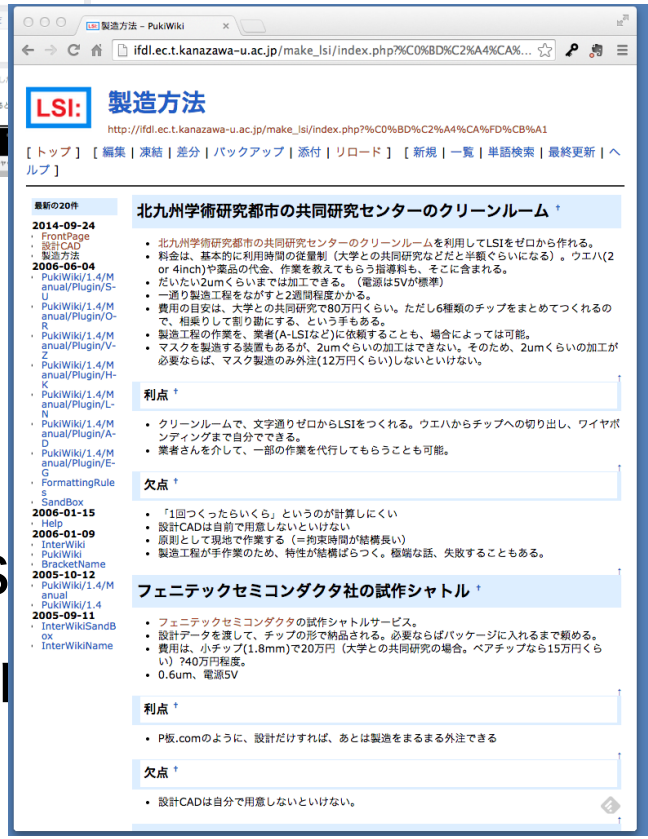
MakeLSI: project by Prof.Akita

- NDA Free VLSI fabrication
  - Search fabrication company without NDA
  - Migration from virtual layout to NDA based one
- VLSI making community
  - Mutual support between users
  - Collect use cases with FOSS or free to use EDA tools

Slides from Prof. Akita will be

MakeLSI: - Outline

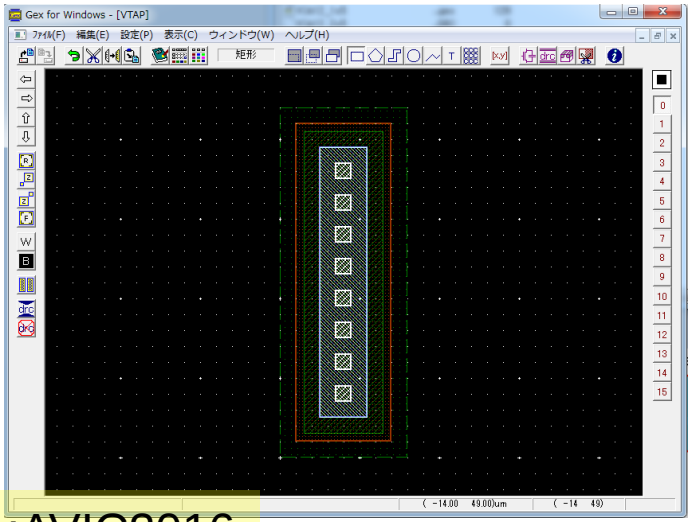
- Know-how Sharing
  - Freeware CAD
  - Basic Knowledges
- Community
  - 100+ in ML
  - LSI Specialists & Non-specialis
  - No Qualification for Contributio
- NDA-Free Fabrication
  - Lambda-rule ～1[um]



http://ifdl.jp/make_lsi

MakeLSI: - Tools

- Layout Tool: Wgex by Prof. Asada @ U.Tokyo
  - Circuit Extraction & DRC
- Circuit Simulator: LTspice / Spice3
- Logic Synthesize & P&R: Alliance
- Commonly Used in Project
  - Sharing Know-hows in usage and design
  - Integrating & Sharing IPs

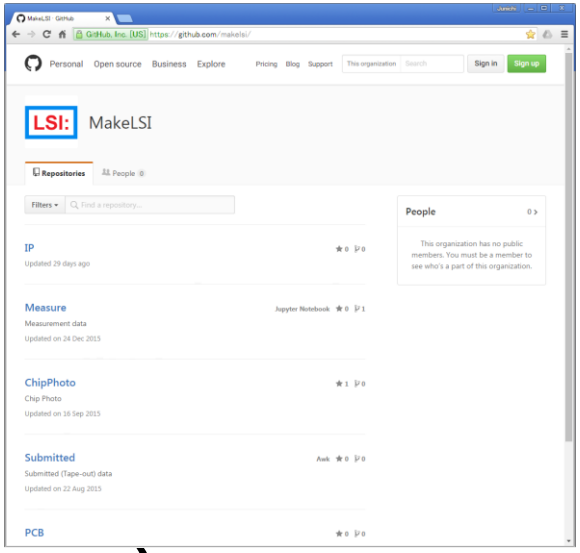


MakeLSI: - Fabrication

- Fabrication Trials with Multi Chip Project at Kitakyushu's Facilities
  - CMOS 2[um], 2Al Technology, NDA-Free
- (Preparing) Phenitec Semiconductors's Shuttle
  - CMOS 0.6[um], 3Al Technology
  - NDA-Free Design Rule based on Kitakyushu's Rule, shrinking x0.3
- (Future) minimalfab by AIST, Japan
  - 0.5in wafer, Mask-less exposure, 1week TAT

MakeLSI: - IPs

- Sharing on GitHub
  - Standard Logic Cells
  - Analog IPs (OPA, BGR)
  - MOS TEGs
- OSHW (Open Source Hardware)
  - NDA-Free Design Rule
    = NDA-Free IP

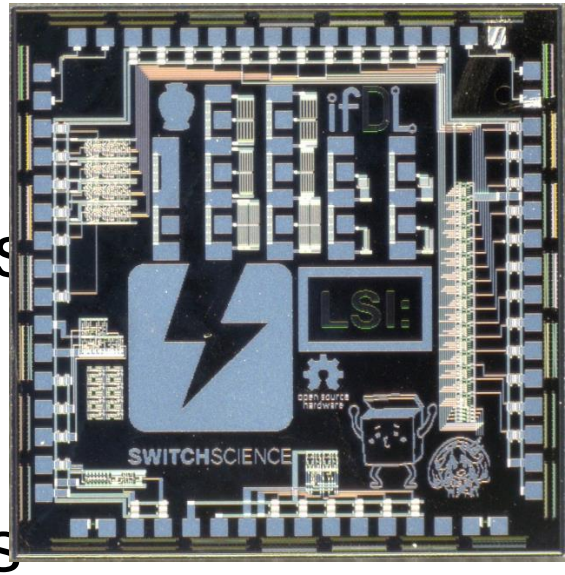


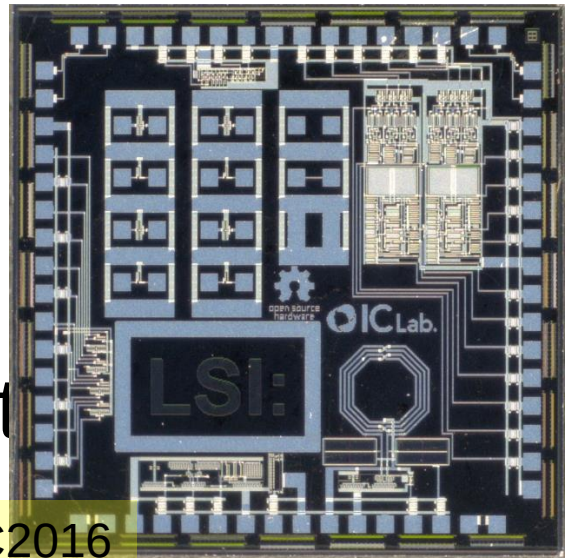
open source hardware

MakeLSI: - 1st Trial in 2015

- 8 Contributors
  - Free fee, Open & Share Contents
- 11 Circuits
  - Kilburn Adder
  - Guitar Effector
  - 1bit CPU
  - 4-16 Decoder
  - Ring VCO, LC-VCO, BGR
- Wide Variety, Passionate Activit

☑Saw Oscillator
☑OPA
☑MOSFET TEGs
☑Timer“555”

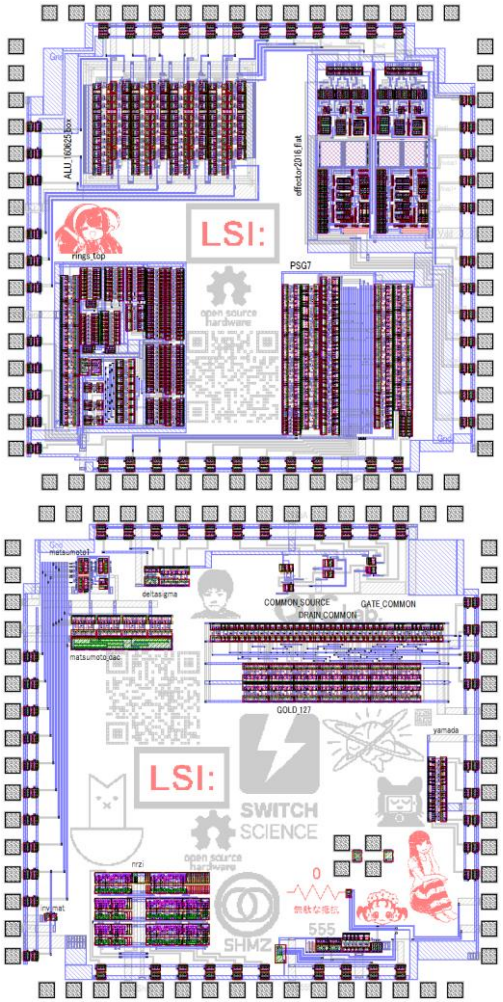




MakeLSI: - 2nd Trial in 2016

- 11 Contributors
  - Free fee, Open & Share Contents
- 12 Circuits
  - ALU
  - Guitar Effector
  - RingOSC
  - PSG
  - Delta-sigma ADC

☑R-2R DAC
☑NRZI Codec
☑GoldCoder
☑Inverter, FA
☑Timer“555”



- Wide Variety, Passionate Activity

Distributed IP Development

- Framework=NDA-Free, Common-Technologies/Tools
- Rapid IP Development
  - Developed by lots of contributors
  - Possible Low Quality (bugs, errors, …)
  - Quality can be improved by contributors,
- Cf. OSS (Open Source Software; Linux, etc.)
  - Quality will be rapidly improved by contributors
  - Contributors' passions for development & improvement (user community)
  - Open framework (source code, license, …)required

Our Challenge

- Use NDA free fabrication
- Use symbolic layout as a virtual layer
- Make our own virtual PDK
  - Prof. Akita used FAIS's as a virtual PDK
    - FAIS rules are too difficult because of process stability
  - New virtual 1μm rules is written by community

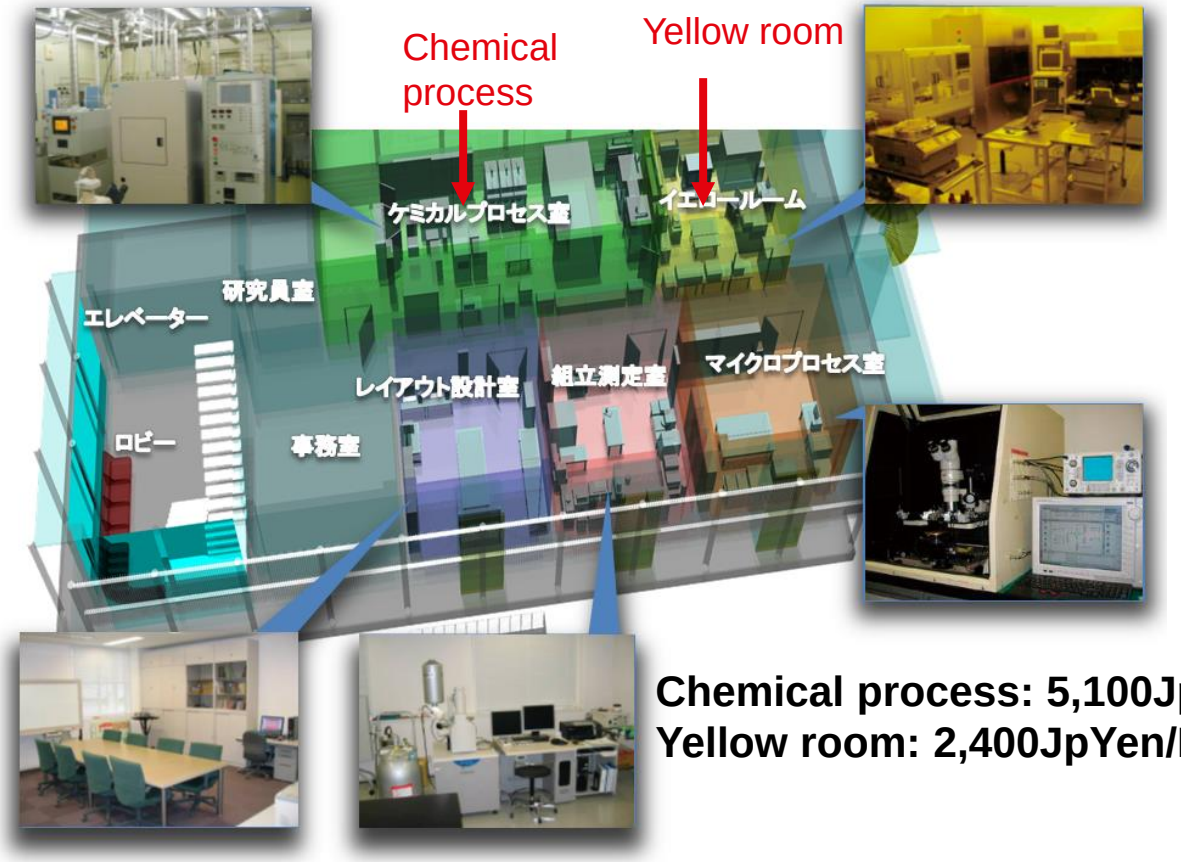
NDA free fabrication

- Kitakyushu FAIS fabrication
  - 2μm old tech. without NDA
  - Based on this technology Prof.Akita organizes “MakeLSI:” community.
- MOSIS SCMOS
  - Scalable CMOS design rules available
    - MOSIS will convert GDS for vendor rules
    - Currently only 0.5μm ON Semi process is available.

Kitakyushu FAIS VLSI foundry

- FAIS provides OLD, but NDA free, low cost CMOS fabrication opportunity
- 2.0μm 2M

We start our efforts with this fabrication facility



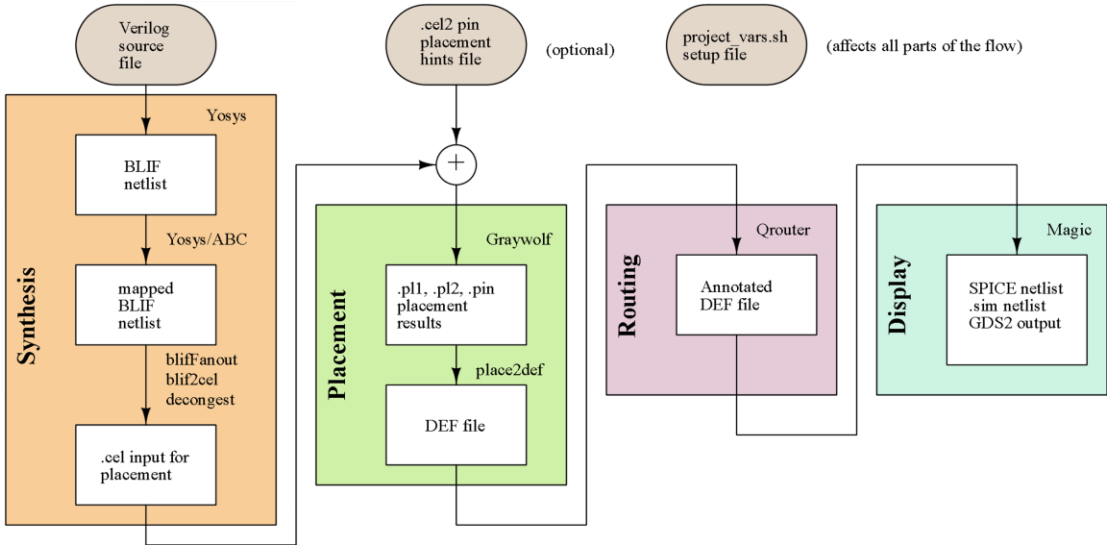
Chemical process: 5,100JpYen/H
Yellow room: 2,400JpYen/H

Symbolic layout efforts

- Lambda rules
  - Based on scaling theory back to Mead and Conway 1981.
    - Every rules are denoted based on the unit lambda.
  - MOSIS provides SCMOS Rules publicly
- Alliance from UPMC, France symbolic rules
  - Lambda with micron based modification
  - Symbolic segments will be converted with multiple segments with database
    - NDA segments can be hidden from symbolic layer.

Symbolic Layout Tools

- Qflow
  - Verilog entry
  - Place/route
  - STA
  - SCMOS rules
  - GDS2 output
  - OSU standard cells for AMI 0.35μm
- Alliance/Coriolis

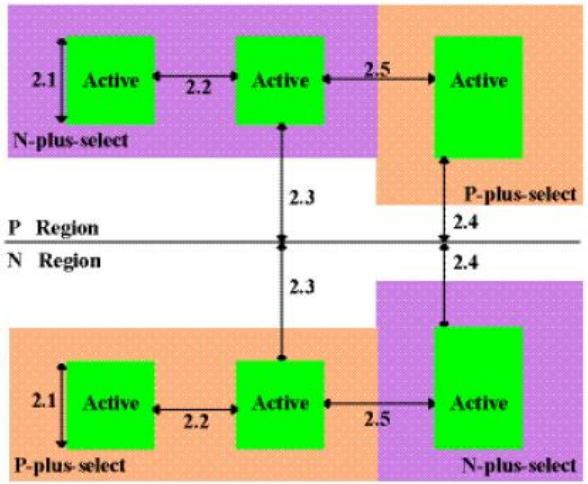


SCMOS Rules

- MOSIS settles SCMOS design rules.
  - The rules is open and published on their web.
  - The rules described on lambda as below.

SCMOS Layout Rules - Active

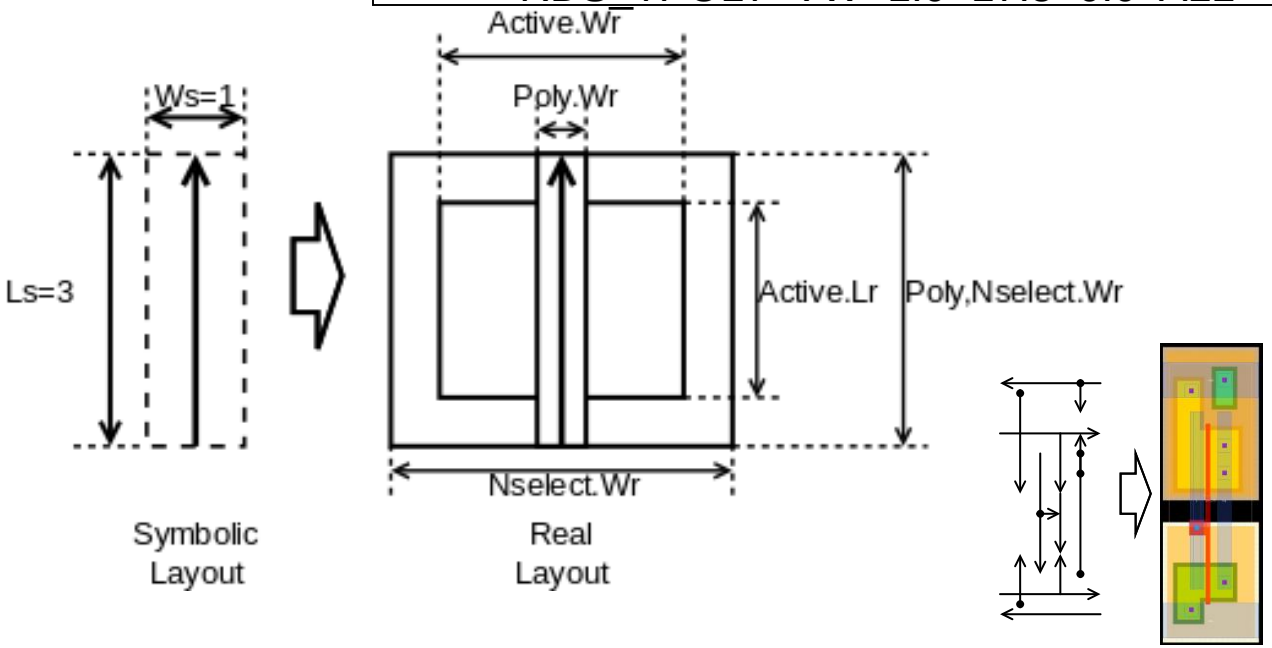
Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
2.1	Minimum width	3 *	3 *	3
2.2	Minimum spacing	3	3	3
2.3	Source/drain active to well edge	5	6	6
2.4	Substrate/well contact active to well edge	3	3	3
2.5	Minimum spacing between non-abutting active of different implant. Abutting active ("split-active") is illustrated under Select Layout Rules.	4	4	4



Alliance:
Symbolic to real layout translation

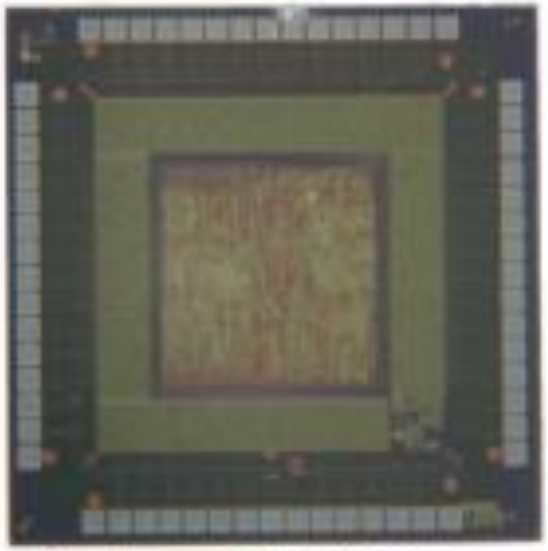
- NMOS Transistor translation example
- Layers
  - Poly
  - NDIF
  - Active
  - Implant
  - Vth imp.

```
NTRANS  RDS_POLY   VW  0.0  -0.5  0.0  ALL \
        RDS_NDIF  LCW -3.0  7.0  -0.25  EXT \
        RDS_NDIF  RCW -3.0  7.0  -0.25  EXT \
        RDS_NDIF   VW -3.0  13.5  0.0  DRC \
        RDS_ACTIV  VW -3.0  13.5  0.0  ALL \
        RDS_NIMP   VW -1.0  17.5  0.0  ALL \
        RDS_TPOLY  VW -1.0  17.5  0.0  ALL
```

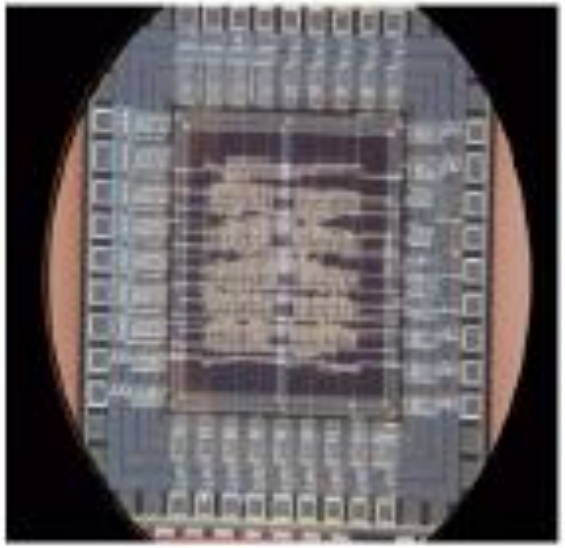


My Chips fully layouted with Alliance

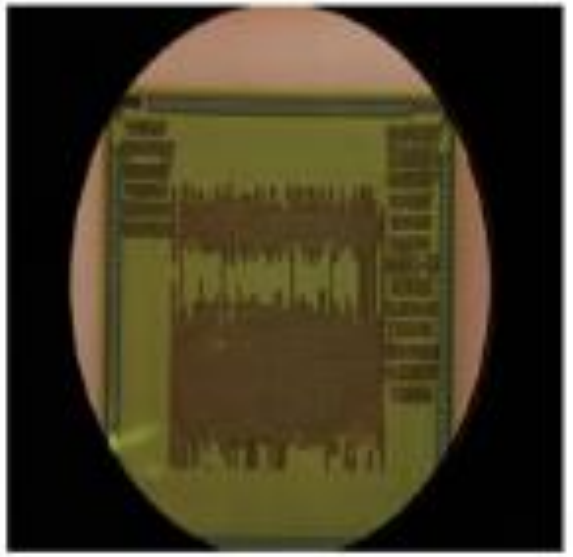
- All these chips are fabricated with VDEC shuttle. http://www.vdec.u-tokyo.ac.jp/



Rohm 0.35um



Onsemi 1.2 um



Rohm 0.18um

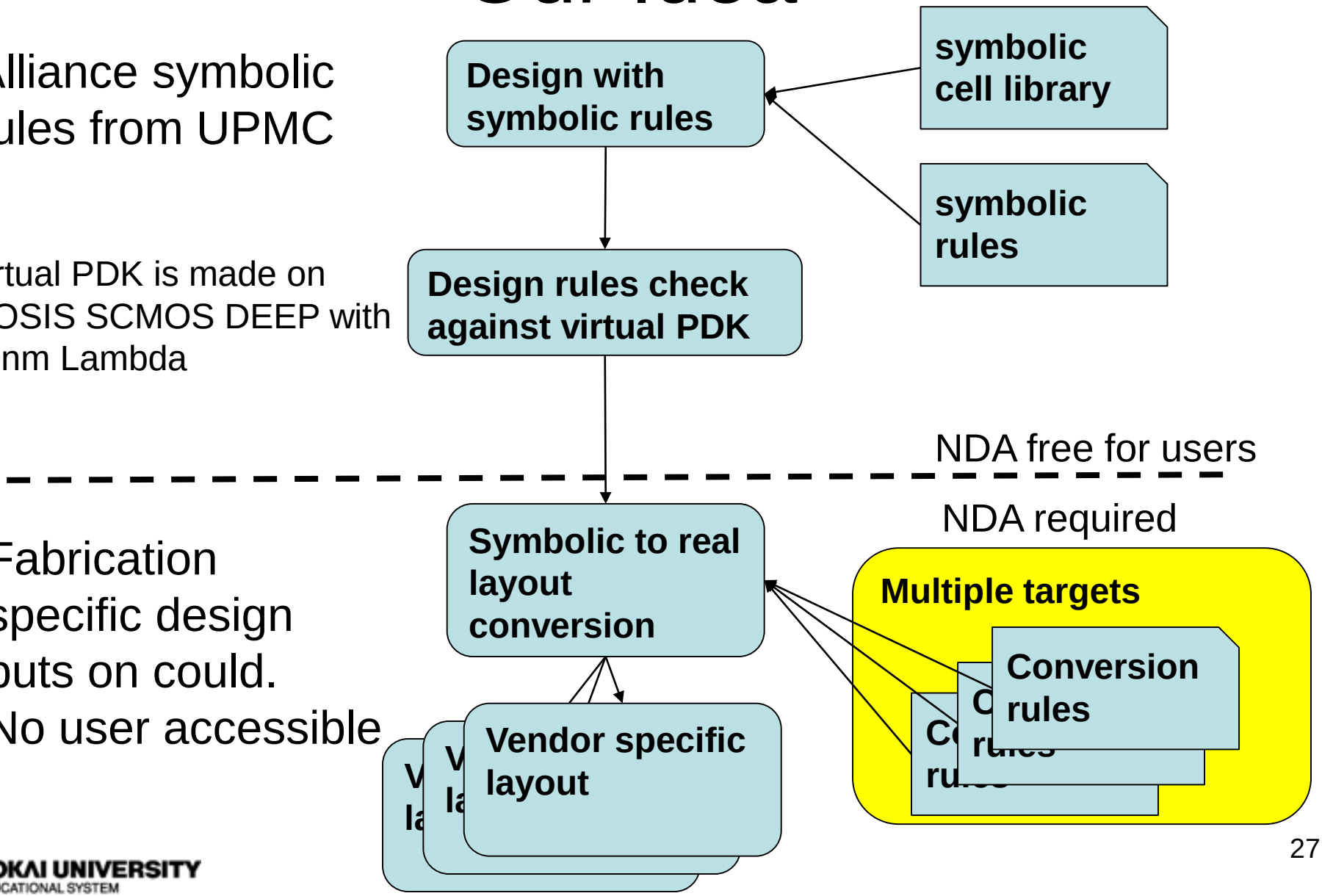
We used NDA based design rules for these chips.

Our Idea

Alliance symbolic rules from UPMC

Virtual PDK is made on MOSIS SCMOS DEEP with 90nm Lambda

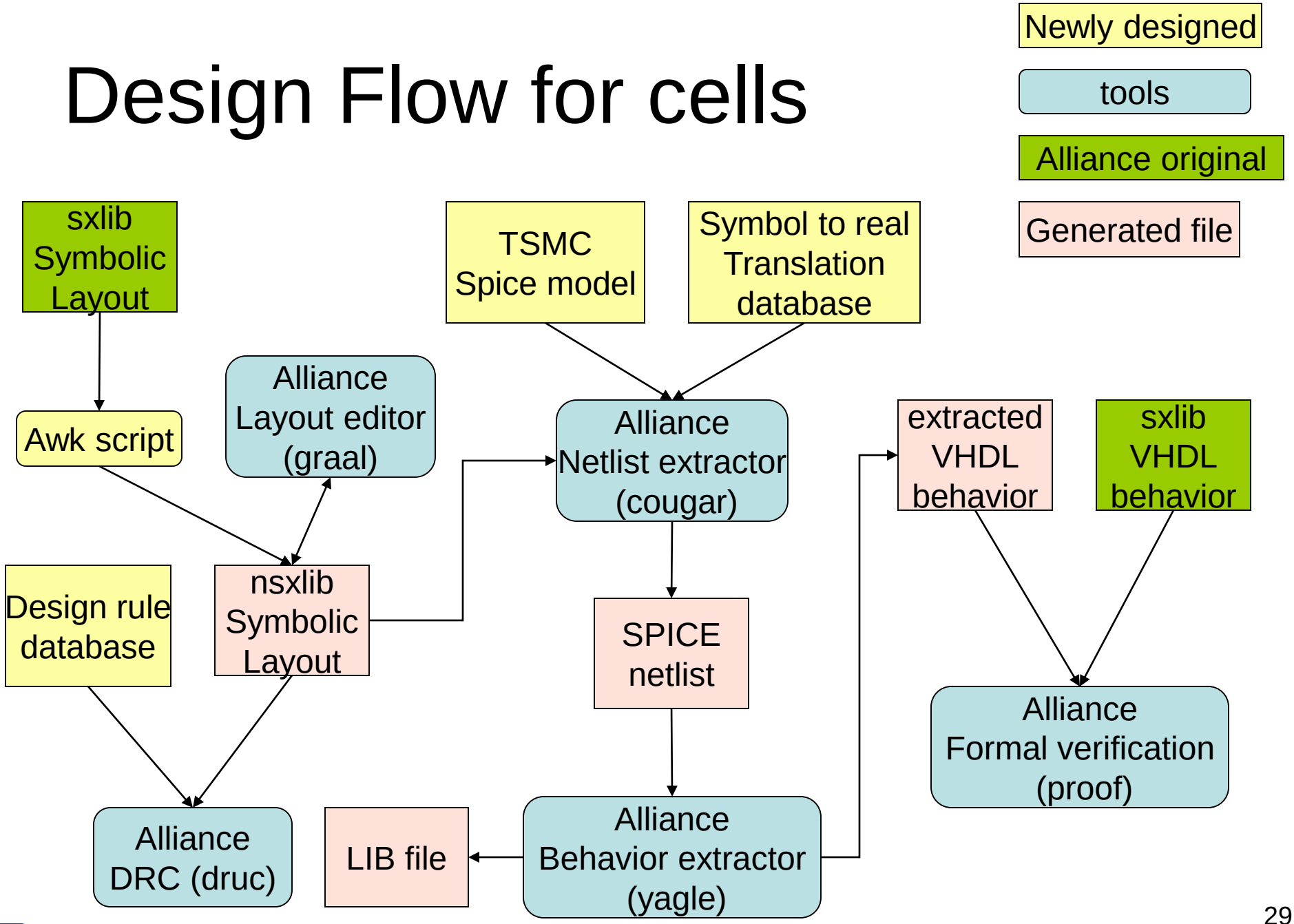
Fabrication specific design puts on could.
No user accessible



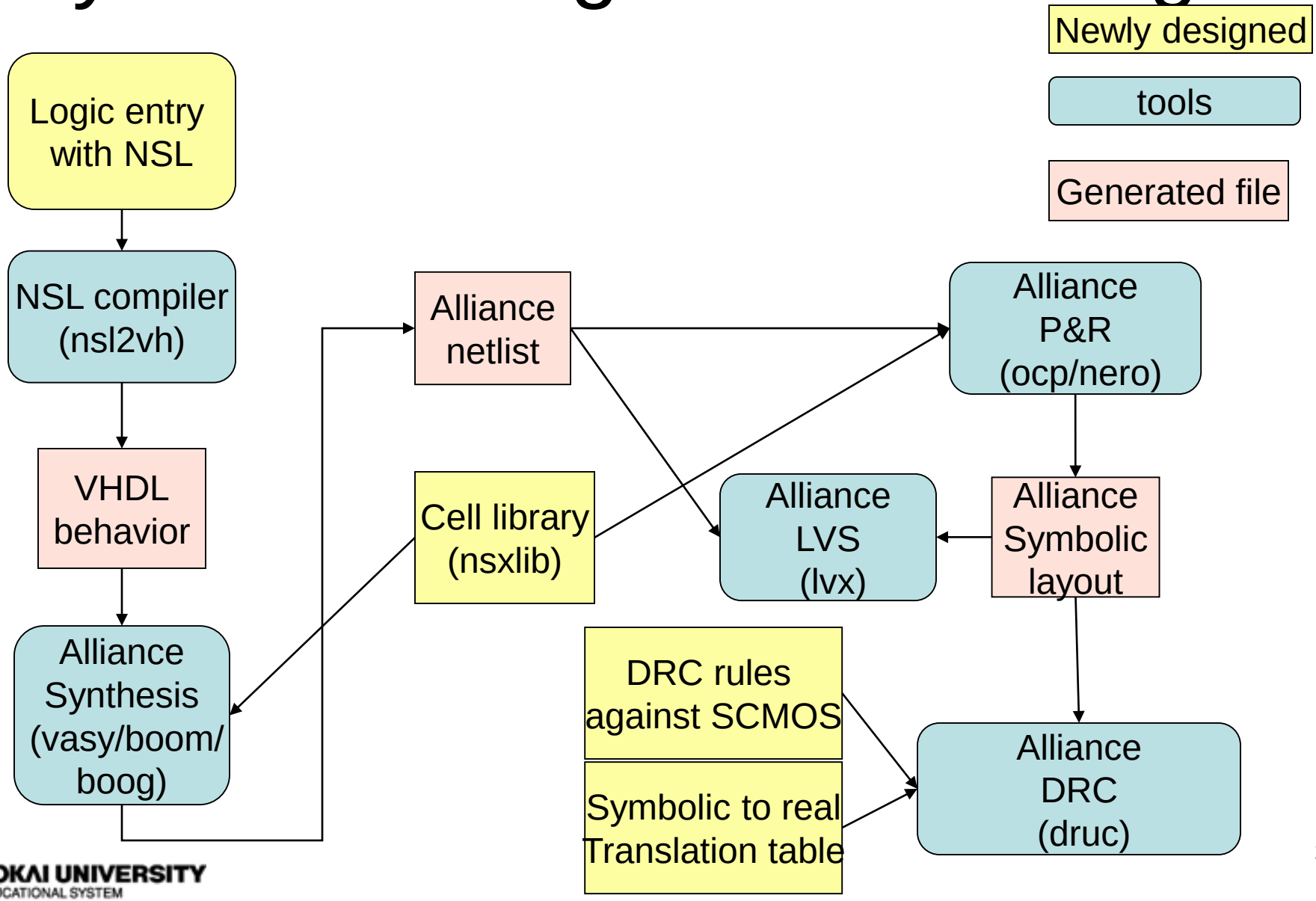
Experiments

- Virtual Layout against SCMOS DEEP
  - Design cell library : nsxlib
  - Write Alliance symbolic to real translation table
  - Write Alliance design rules check deck
  - Write symbolic IO cells
- NDA based real layout
  - Write Alliance symbolic to real translation table
  - Write Alliance design rules check deck
  - Merge vendor frame GDS with generated GDS

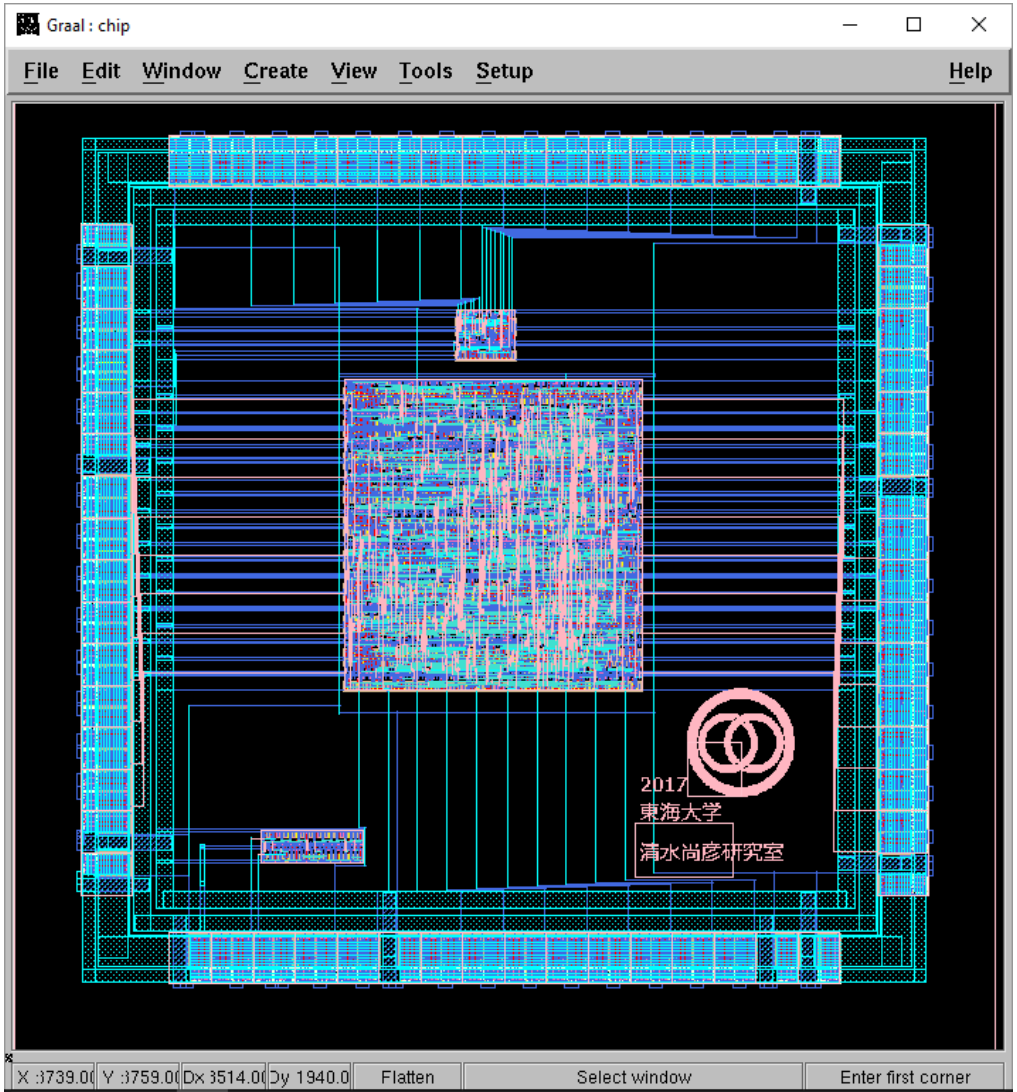
Design Flow for cells



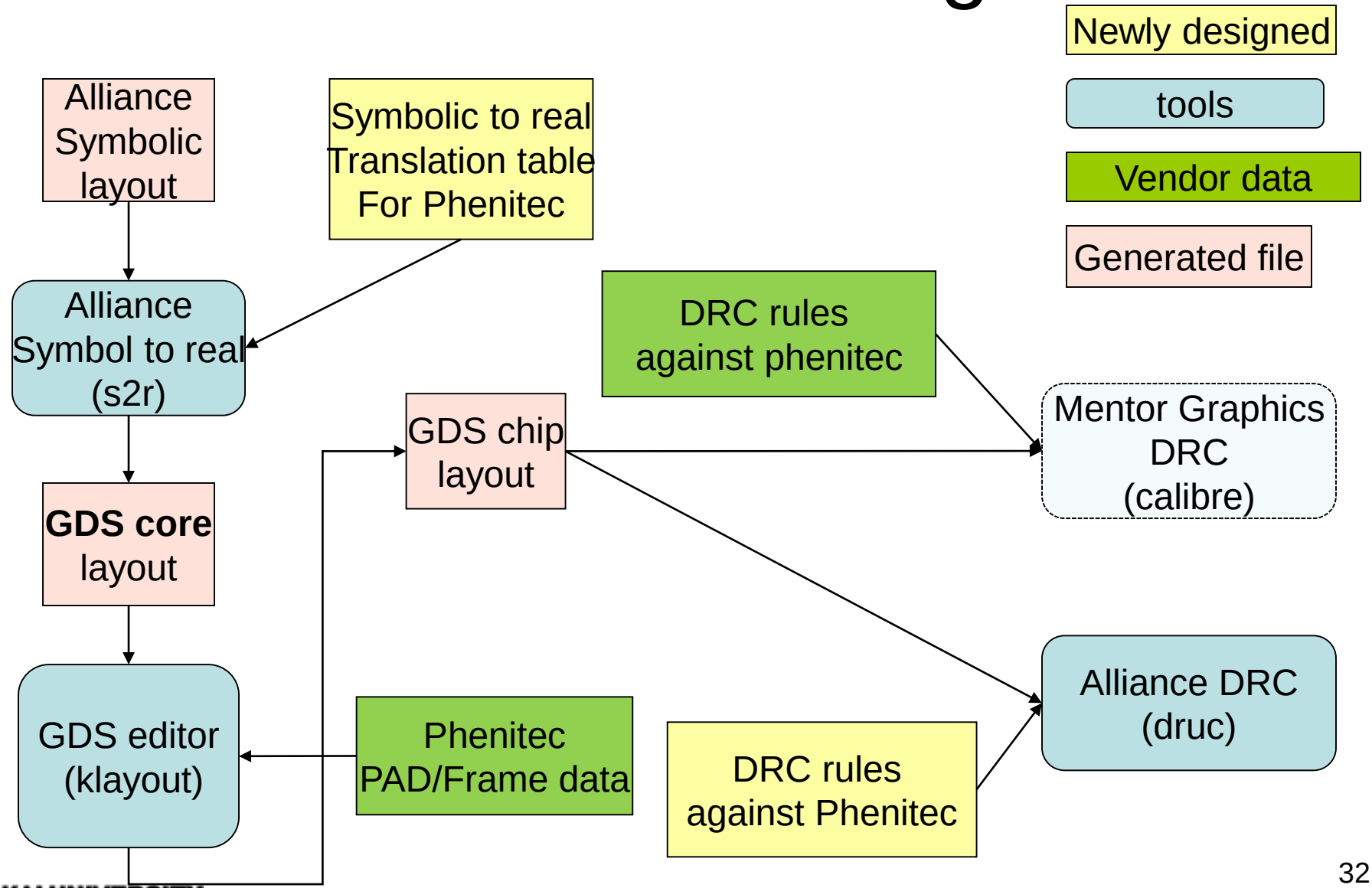
Symbolic Design Flow for Target



Symbolic layout with nsxlib



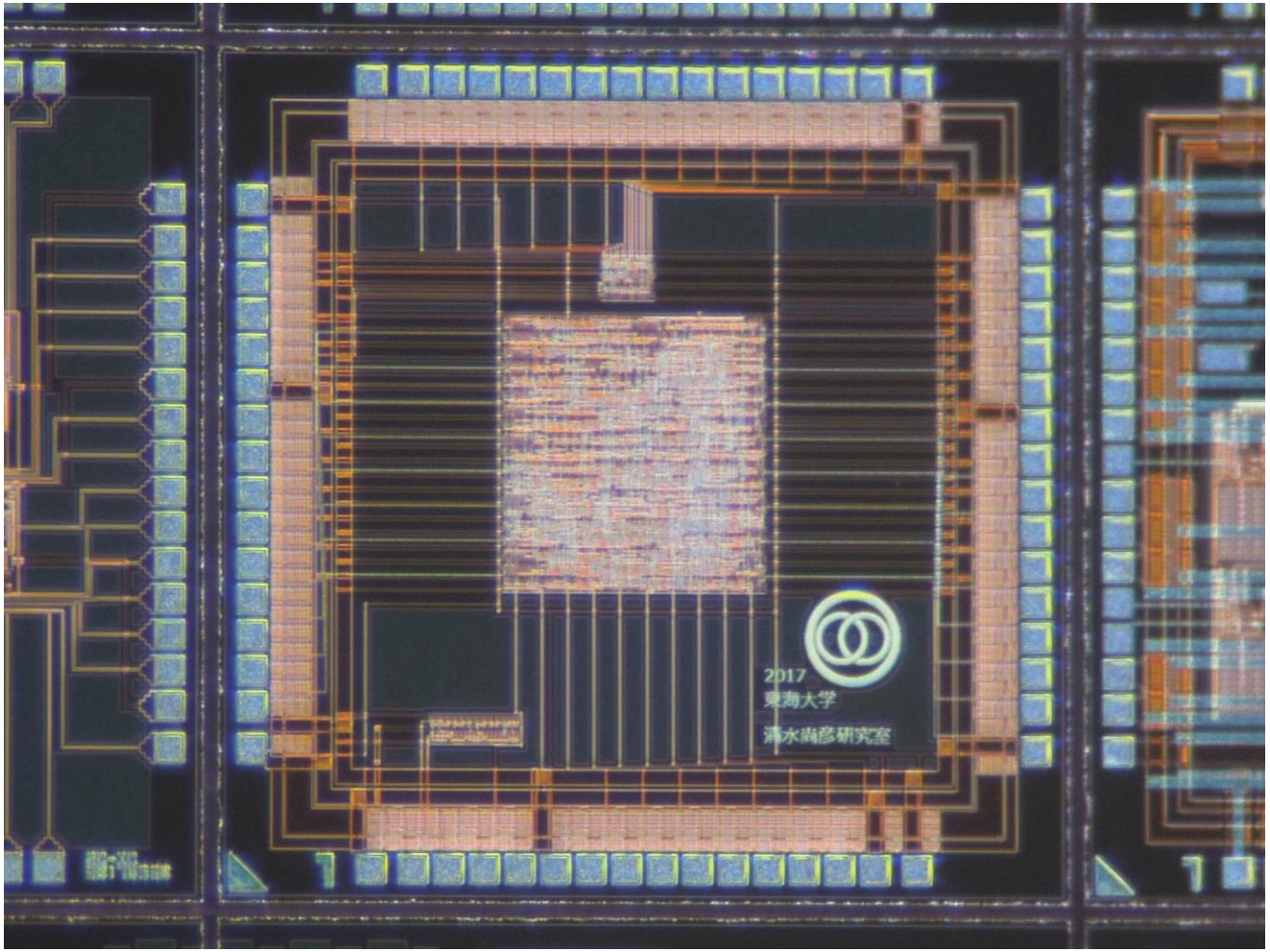
NDA based GDS design flow



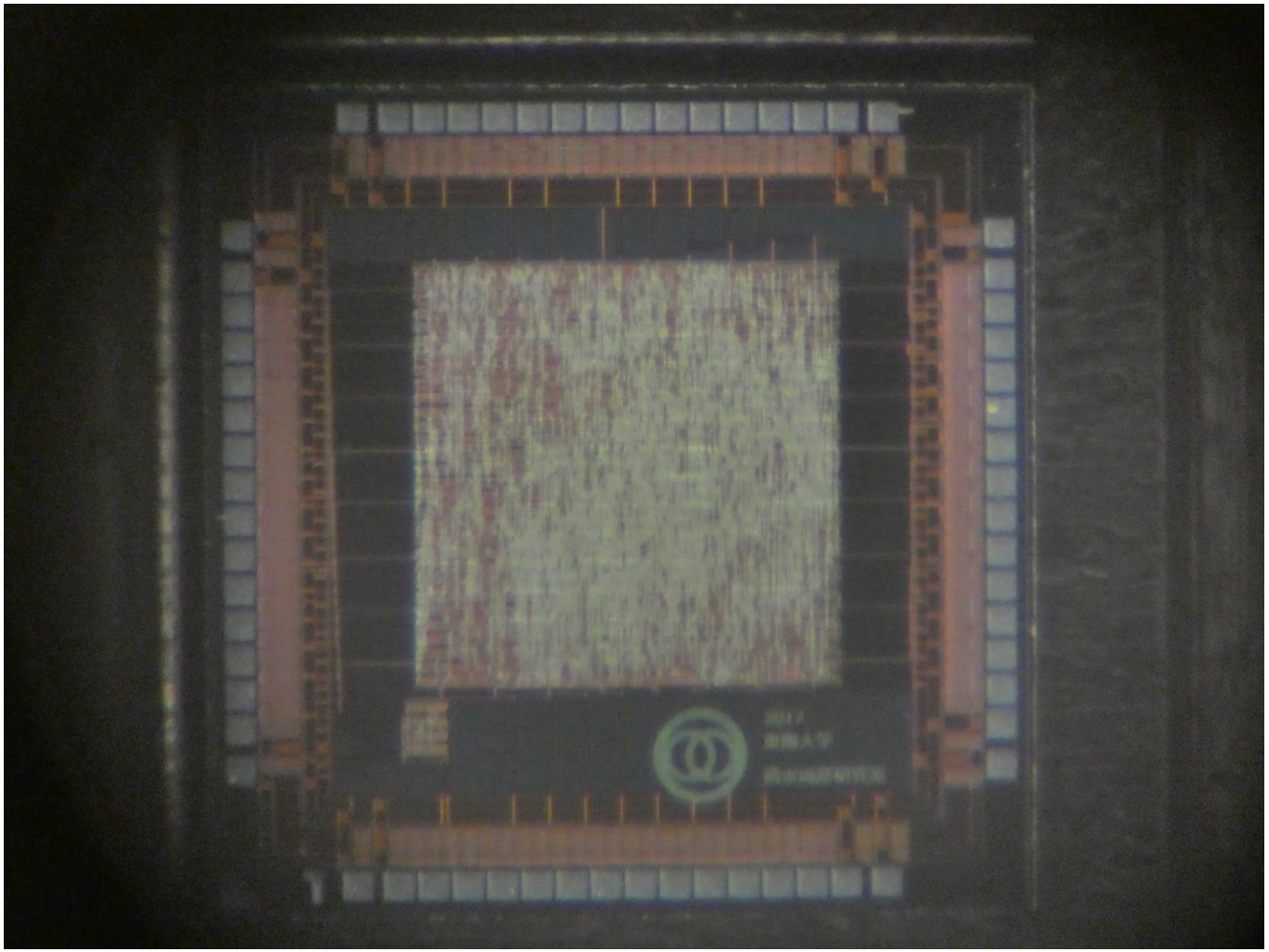
Problems on Phenitec chip

- Phenitec has tighter design rules than SCMOS
  - Adjust ‘nsxlib’ to be compatible with both.
- Alliance could not read the GDS2 for PAD and frame by Phenitec
  - Use ‘klayout’ to merge GDS2s
- PAD alignment is not even.
  - Manually place and route the PADs
- IO cell area is too small! Create new cells.

Fabrication Trial for Phenitec 0.6μm process



Fabrication Trial 2
for Phenitec 0.6μm process



Conclusion

- VLSI design flow and methodology without NDA is proposed
  - fabricated chips with Phenitec 0.6μm process
- We started to discuss on 0.35μm chip with Phenitec
- We are expanding this method for deeper processes.
- Alliance based symbolic layout is practical for our goal.