Systematic Design Procedure for Q-Enhanced Integrated LC Filters

Diomadson Rodrigues Belfort,
Nicolas Beilleau and
Hassan Aboushady
University of Paris VI, Pierre & Marie Curie
LIP6 - SoC Laboratory

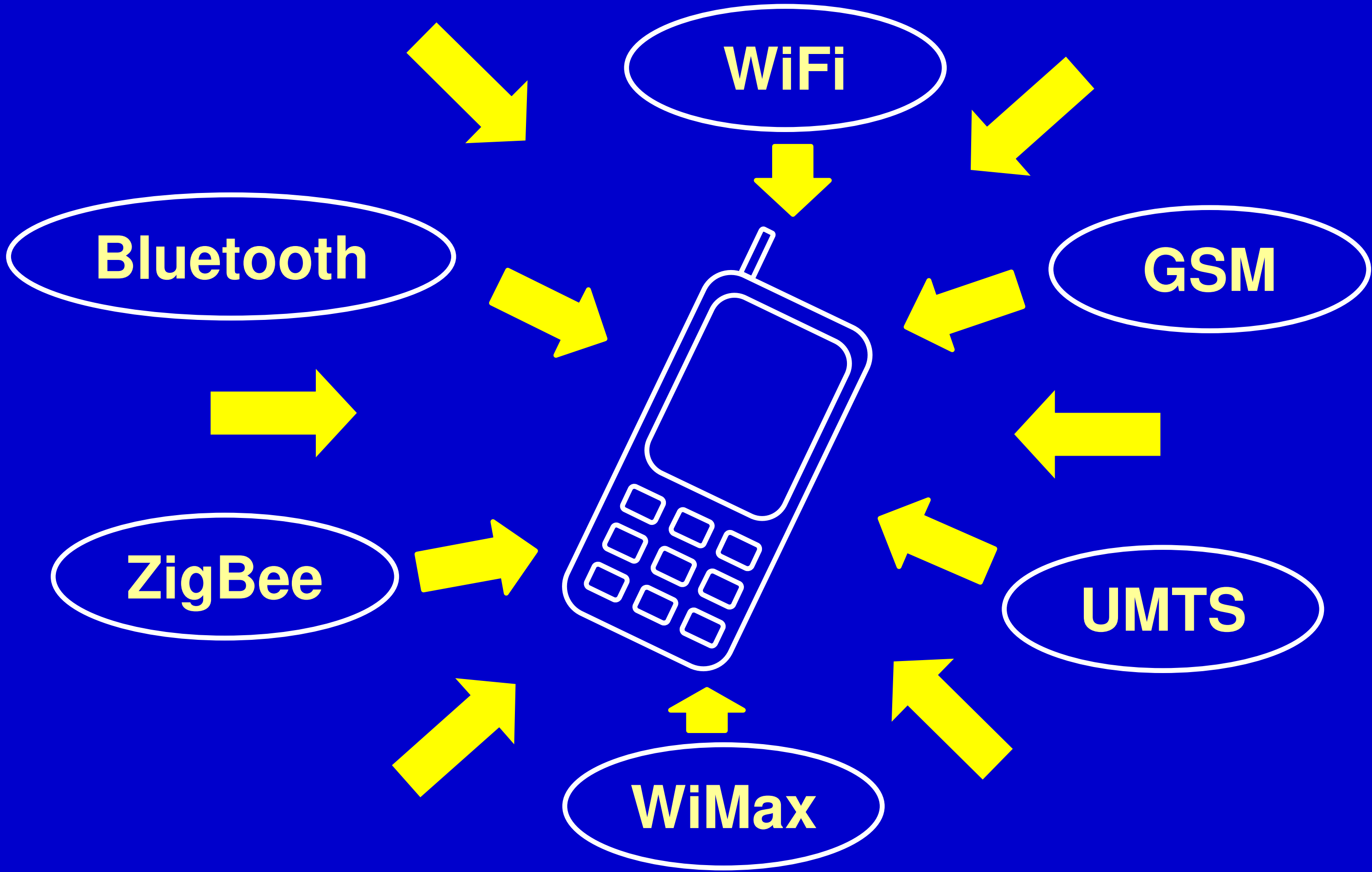
madson@asim.lip6.fr

http://www-asim.lip6.fr/~madson/

Outline

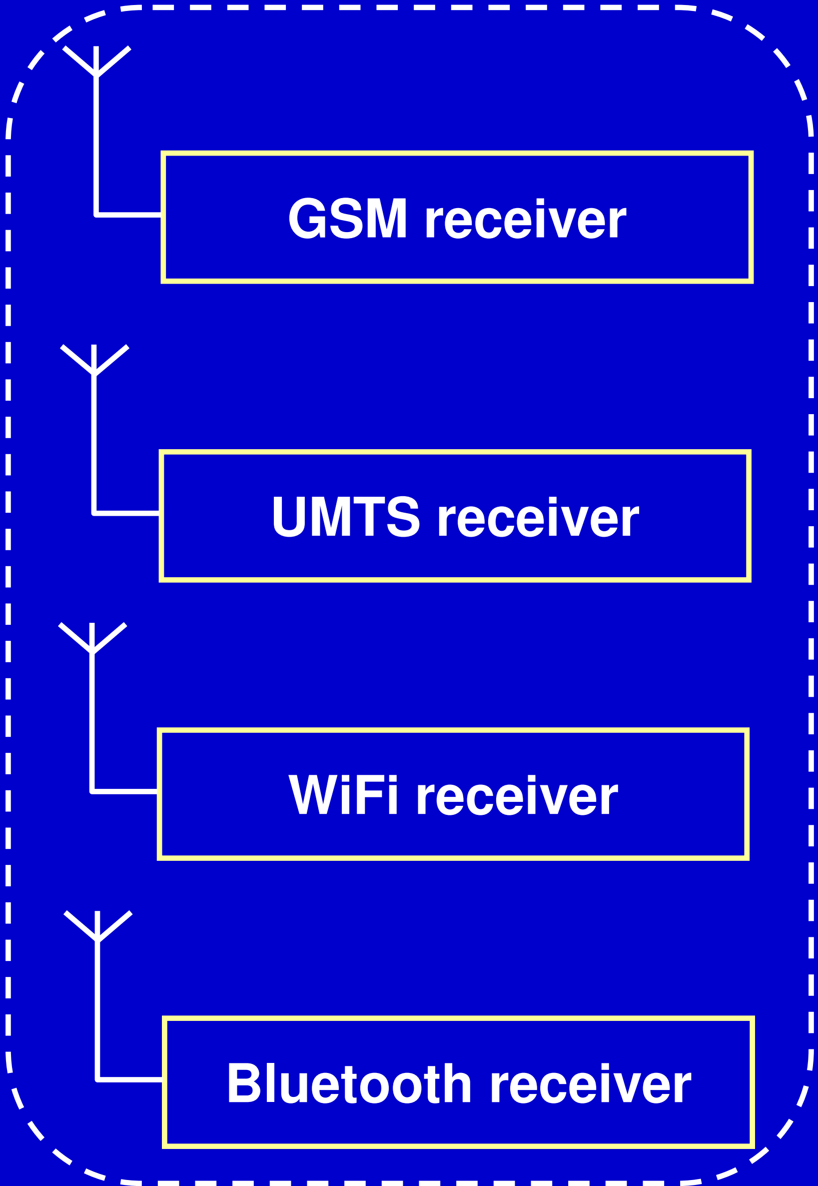
- Introduction
- ΣΔ Modulators
- Differential inductor simplified π model
- Automatic design procedure based on CAIRO+
- Simulations Results
- Conclusion

Digital Communication Wireless Standards



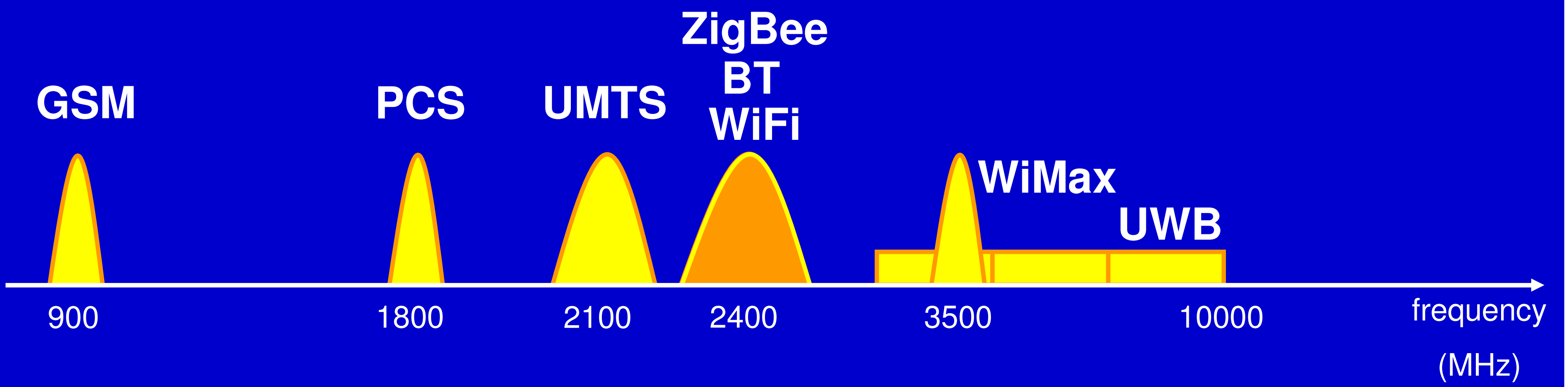
- There are more and more wireless standards for different usage.
- Portable devices need to be compliant with several standards with a limited power consumption.

Several Single-Standards Receivers



- Simple and fast solution to implement.
- Needs a large area.
- Addition of the power consumptions.
- Cost.
- No flexibility.
- Finding a possibility to merge some of the functionalities.

Standards Frequency Bands

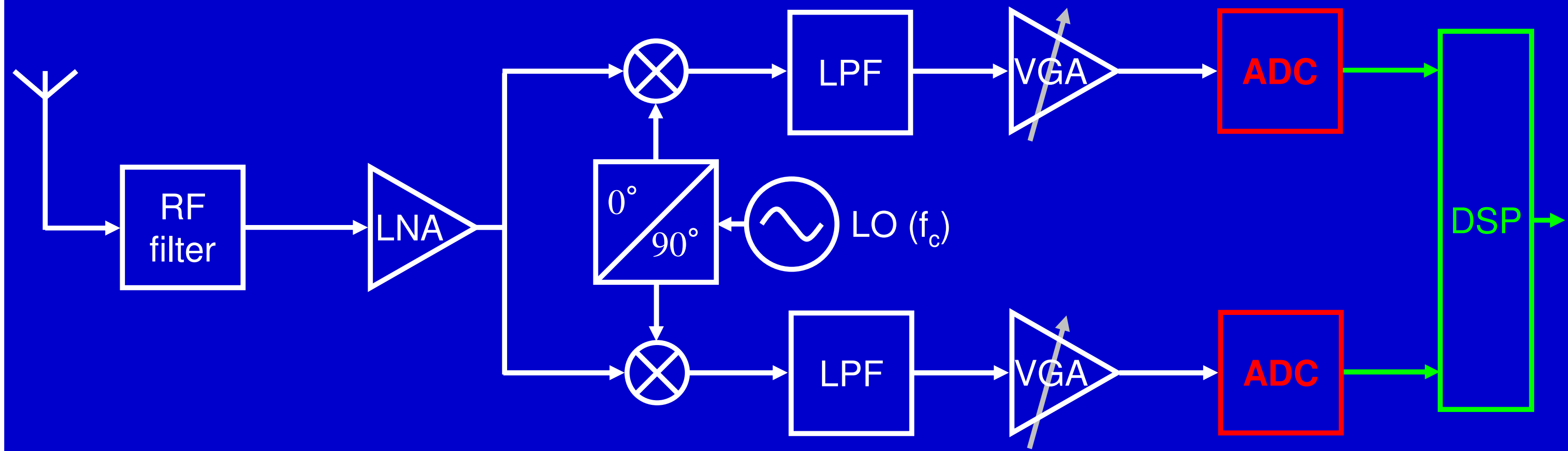


- **Standards are spread over a large frequency band.**
- **Difficult to process all the standards with the same receiver.**

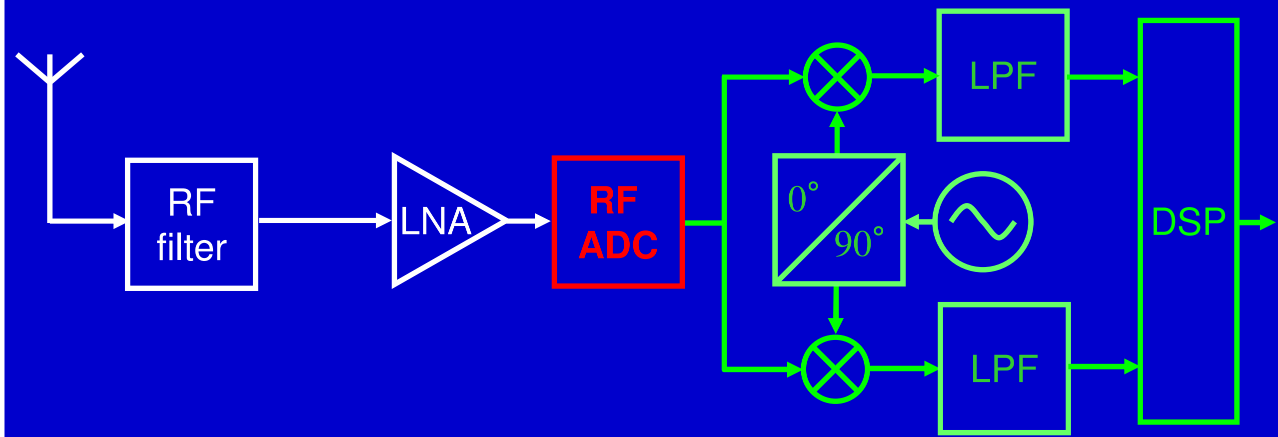
wireless standard	frequency spectrum	channel spacing	data rate
Bluetooth	2400-2484 MHz	1MHz	1Mbps
Zigbee	2400-2484 MHz	5MHz	250kbps
WiFi	2400-2484 MHz	25MHz	54Mbps

Multi-Standard RF Receiver

Conventional Architecture



Architecture based on RF ADC



Advantages:

- Software programmability.
- Digital robustness and technology scaling.

Challenges:

- ADC needs High Dynamic Range.
- Huge Bandwidth to convert.

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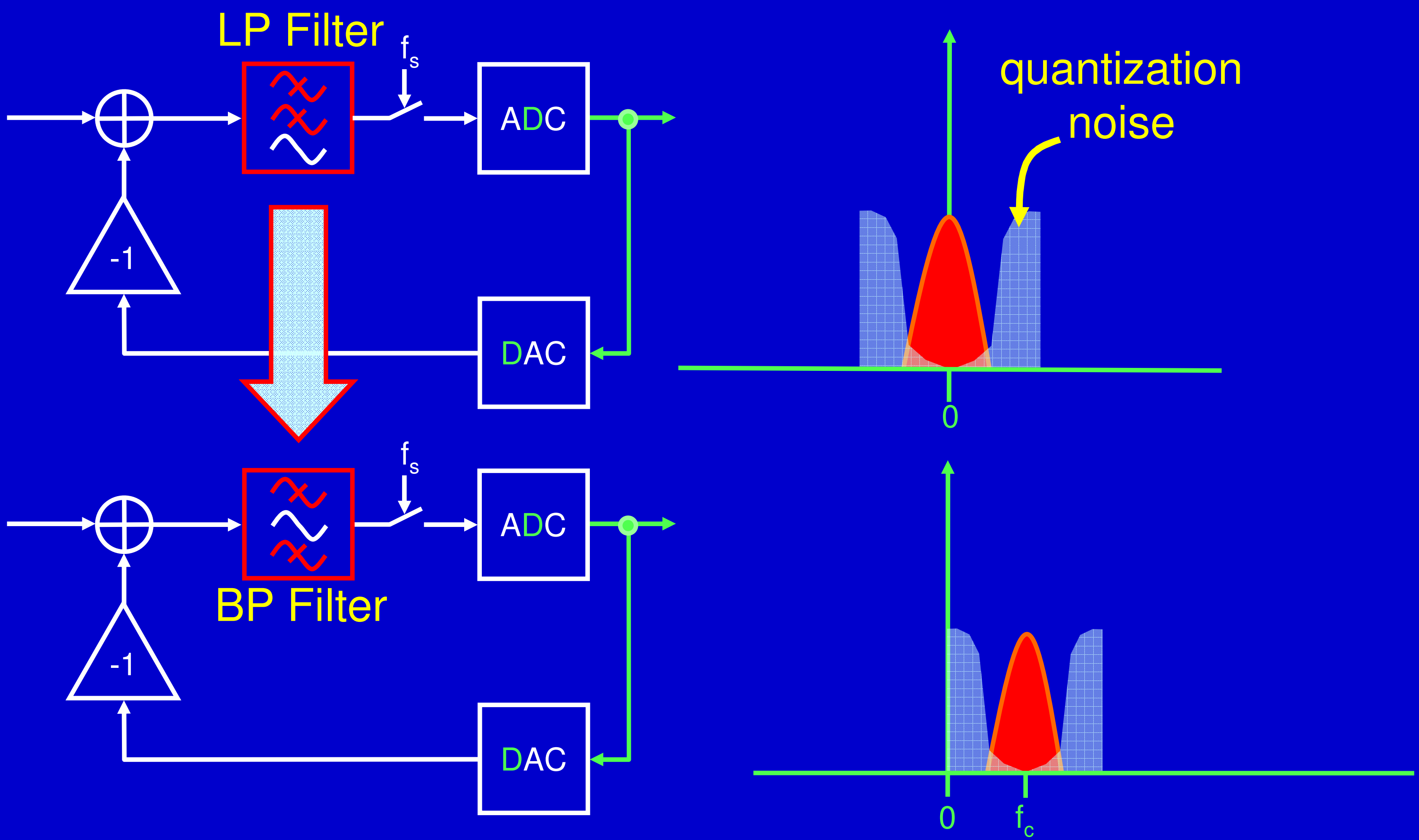
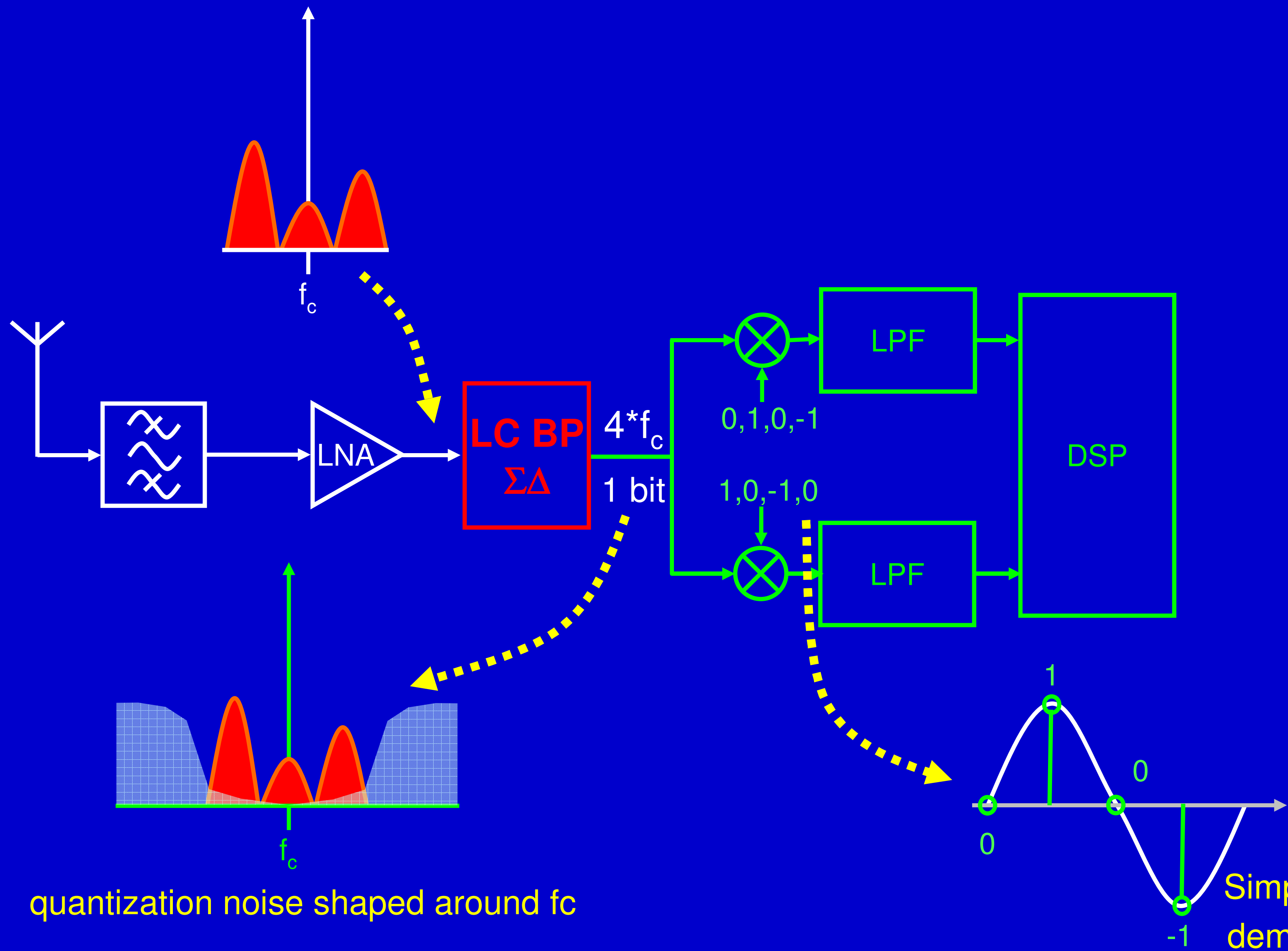
ΣΔ Modulation Technique

Oversampled output signal and ***noise shaping***.



RF LC Bandpass ΣΔ



quantization noise shaped around fc

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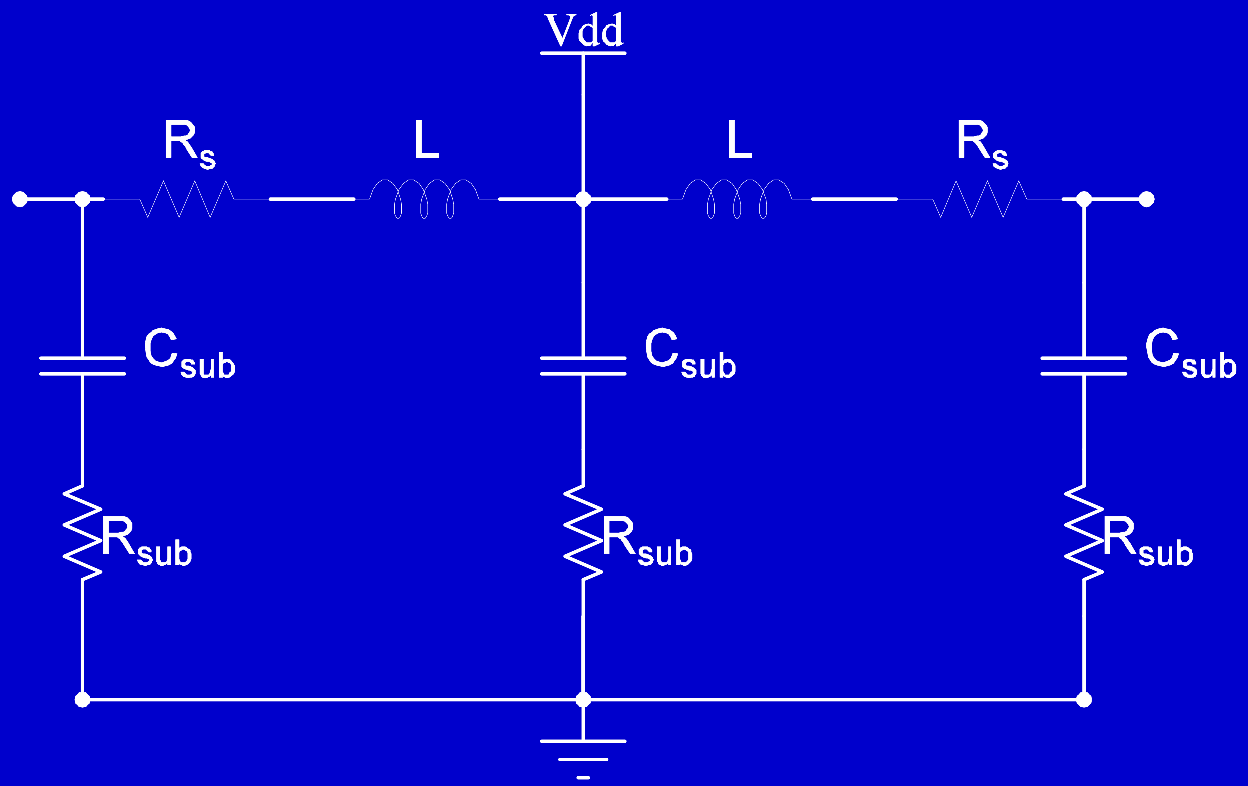
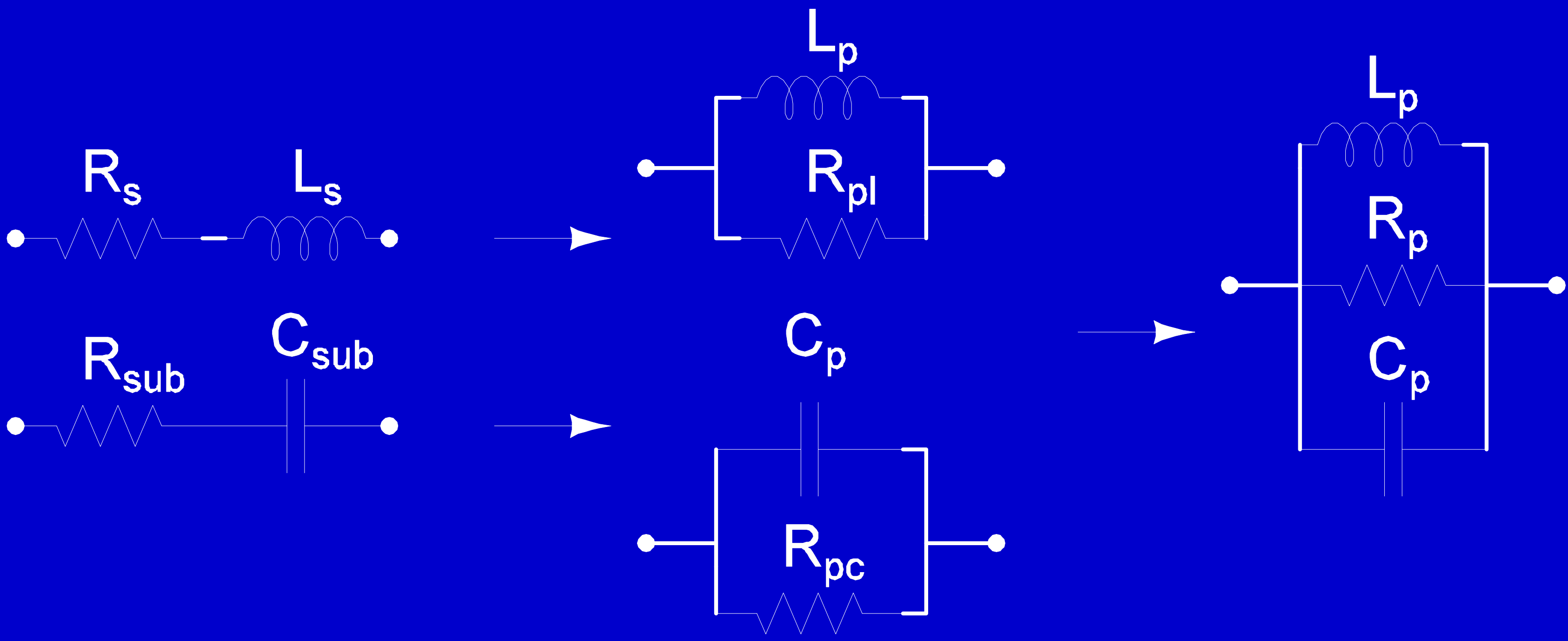
Differential inductor simplified π model



Non-idealities due to the integration of a differential inductor are expressed in an electrical model.

Considering the π model for a differential inductor how can we simplify it to an expression suitable for the LC filter design ?

Parallel transformation of the π model



$$L_p = \frac{1+Q_{ls}^{2}}{Q_{ls}^{2}} L_S$$

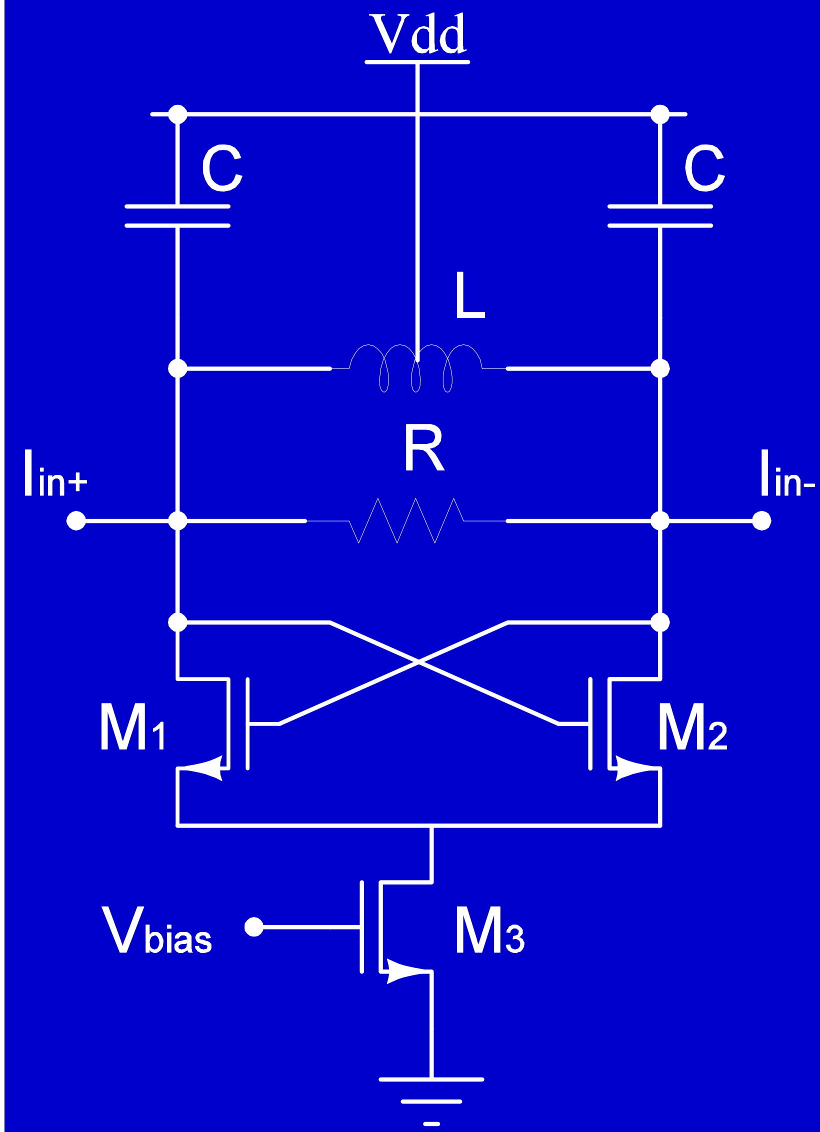
$$C_{sub_p} = \frac{Q_{cs}^{2}}{1+Q_{cs}^{2}} C_{sub}$$

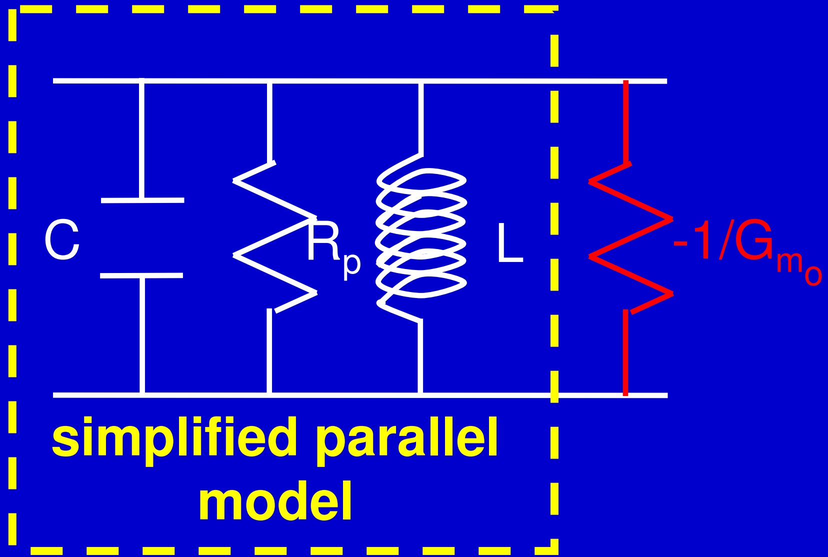
$$R_{p_L} \approx \frac{R_s}{(\omega_o L)^2}$$

$$R_{p_C} \approx \frac{1}{R_{sub}(\omega_o C_{sub})^2}$$

$$R_p = R_{p_L} // R_{p_C}$$

Quality Factor Enhancement





$$Z(j\omega) = \frac{j\omega / C}{(j\omega)^2 + (1 - G_{m_o} R_p)/(R_p C)\, j\omega + 1/(LC)}$$

$$G_{m_o} = G_m - G_{ds} = \frac{1}{\omega_o L}\left(\frac{1}{Q_o} - \frac{1}{Q_{enh}}\right)$$

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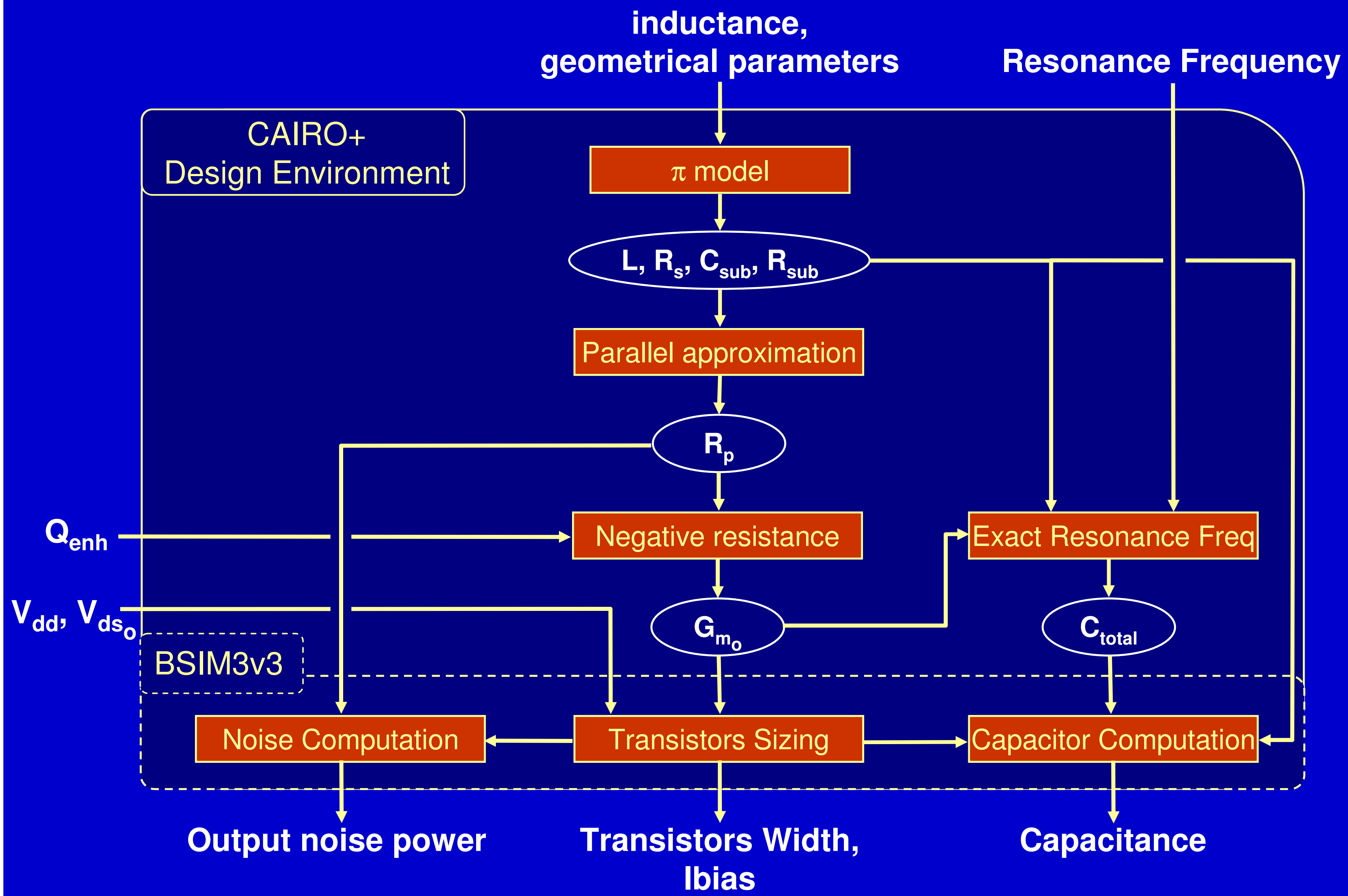
Q-enhanced LC filter design procedure



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LC Filter Circuit Parameters

0.13µm CMOS technology.

$\omega_o = 2\pi f_o$ with f_o=2.442GHz

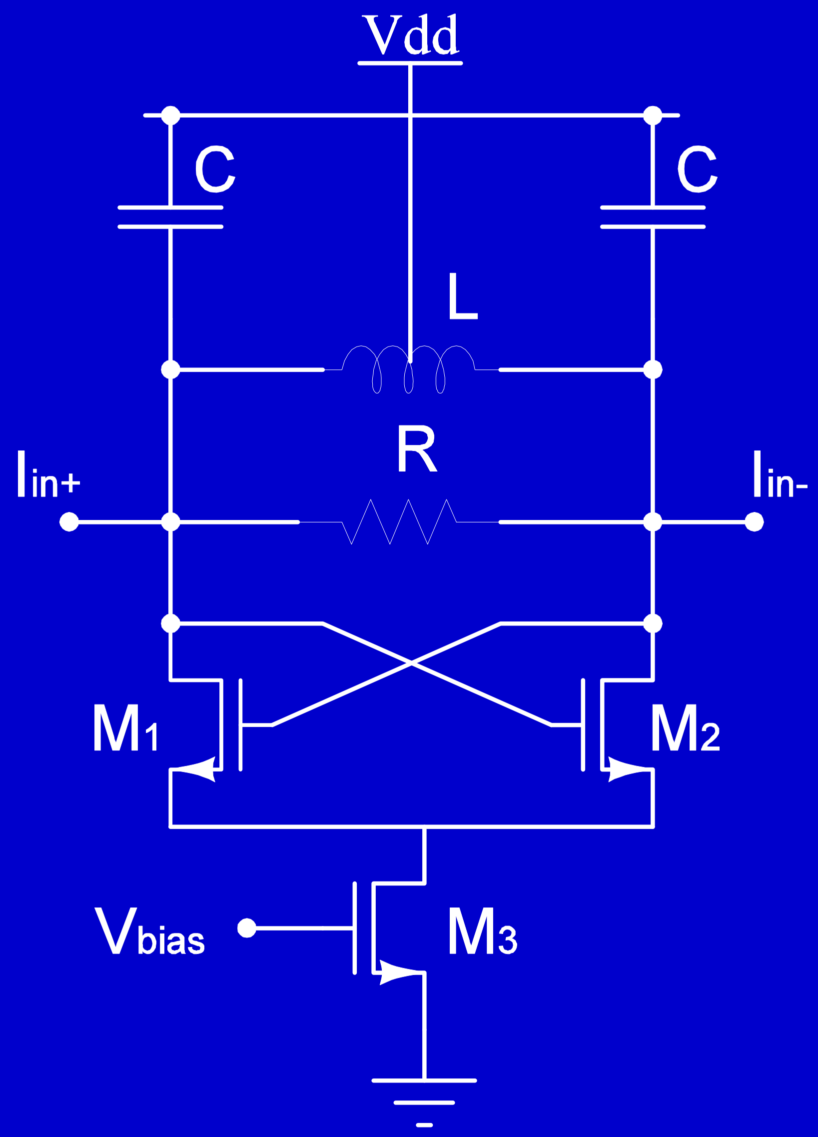
L = 5nH (4 turns, w=12µm, s=10µm)

Capacitors are ideal.

$Q_o = 15$

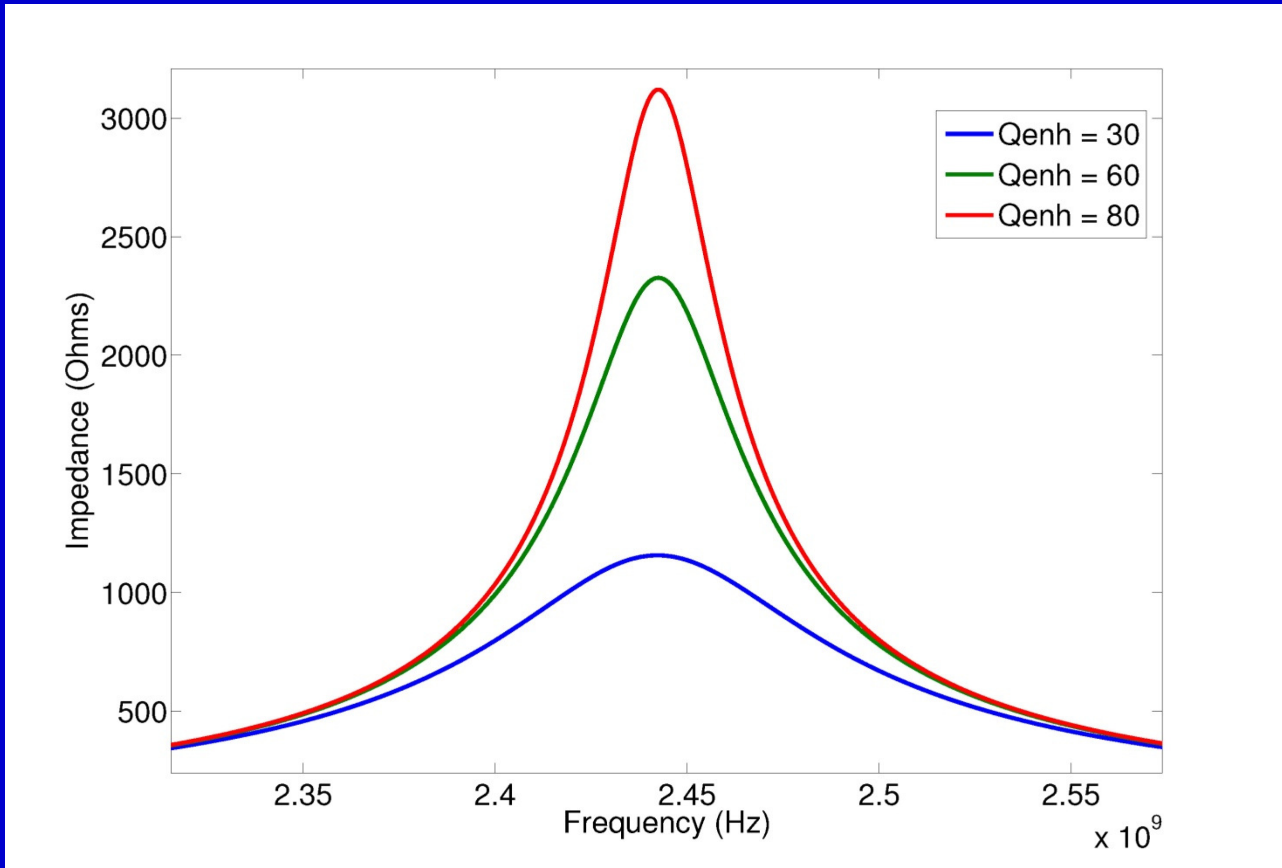
$V_{dd} = 0.6V$ and $V_{ds_o} = 0.3V$

Filter has been redesign for different quality factors.



Total Impedance for different values of Q

CAIRO+ allows to design easily LC filters with different specifications.



CAIRO+ output ***Spice*** netlists are used to verify the generated circuits.

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A systematic design procedure based upon on the inductor π model and the BSIM3v3 transistors model has been presented.

Parallel model of inductor losses for the negative resistance sizing and series model for the capacitance value have been used in the CAIRO+ Design Environment.

Several designs have been presented to demonstrate the validity of this approach.

Thank you !